

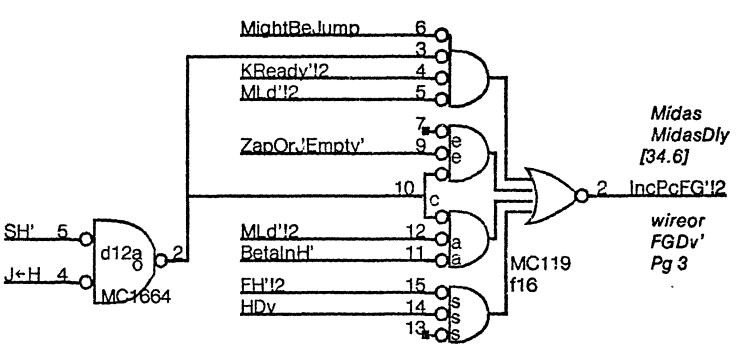
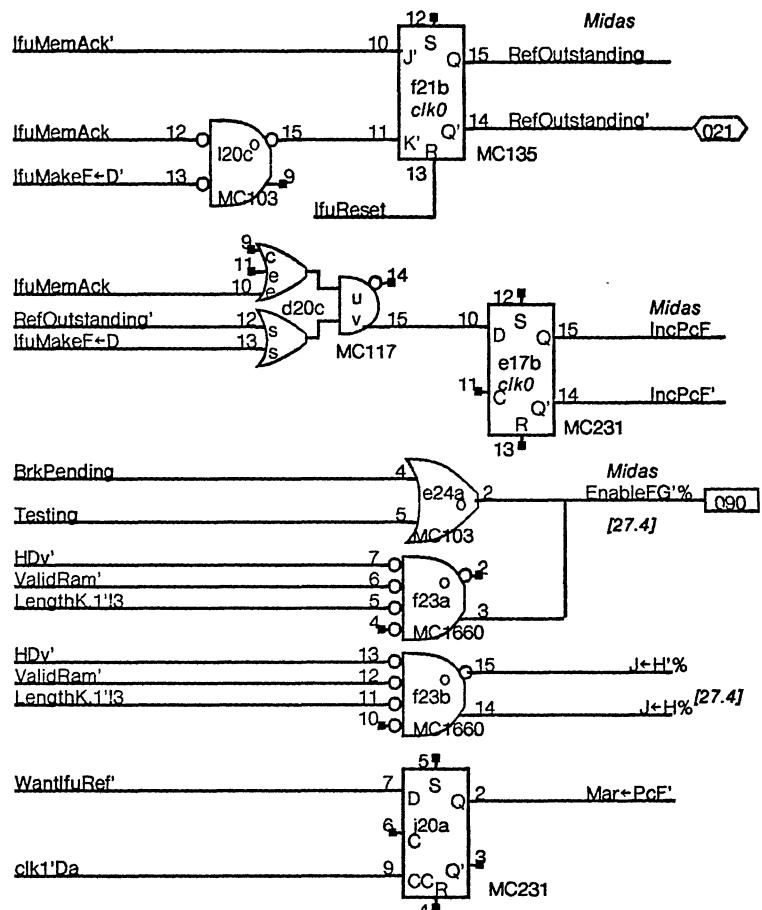
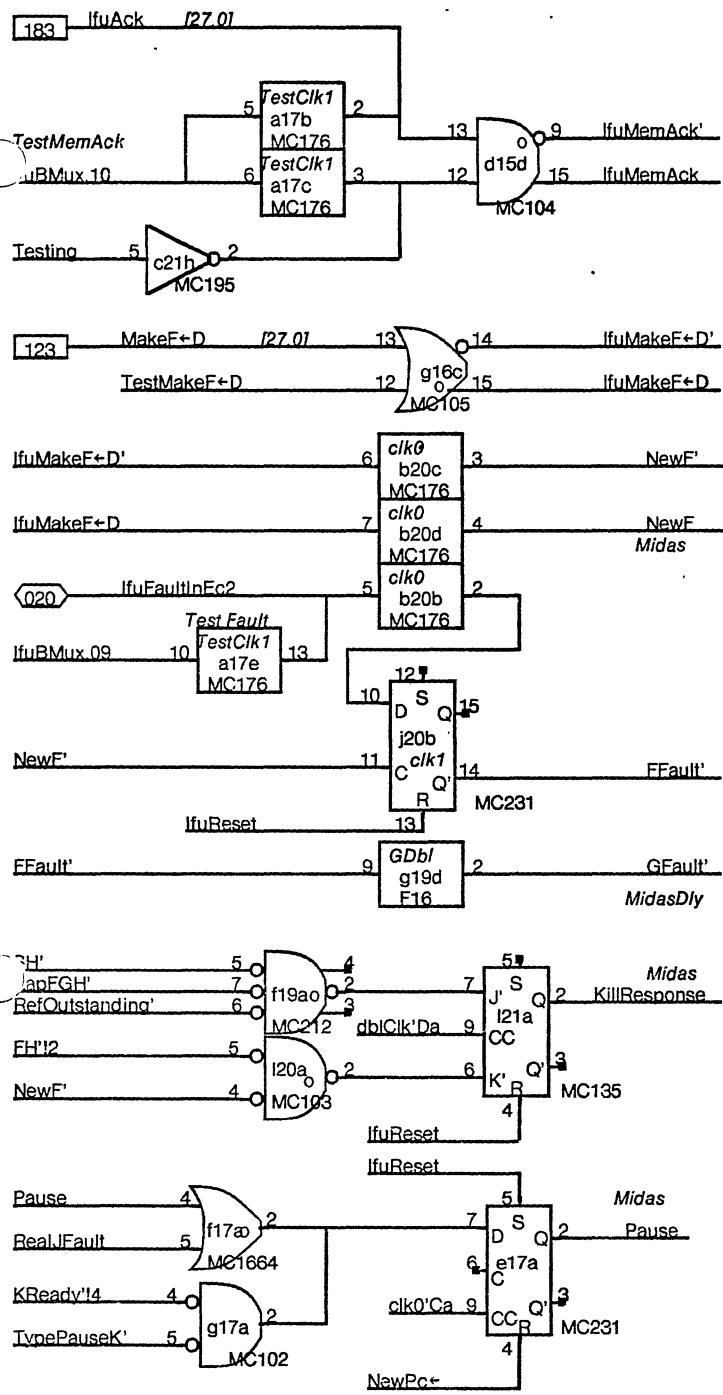
DORADO SCHEMATICS

Instruction Fetch Unit

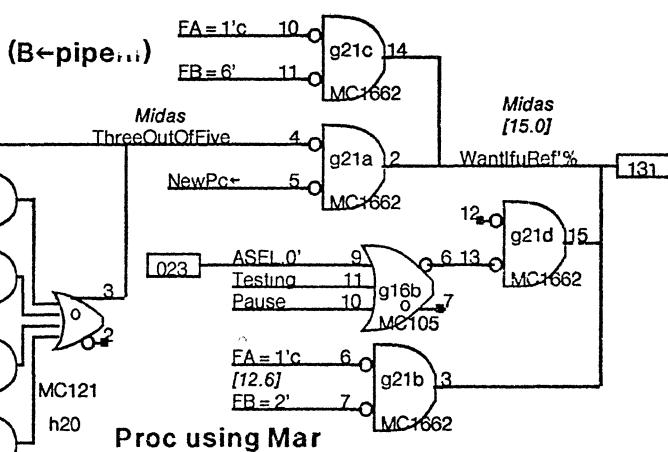
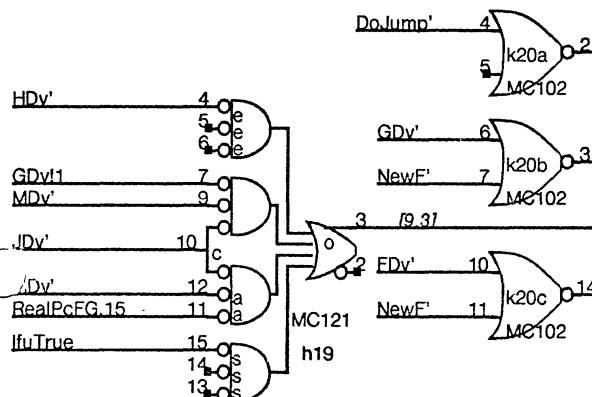
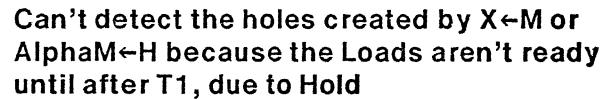
PROM SC 139 - 111 A6

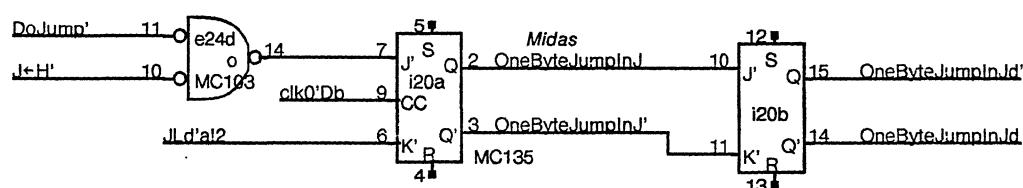
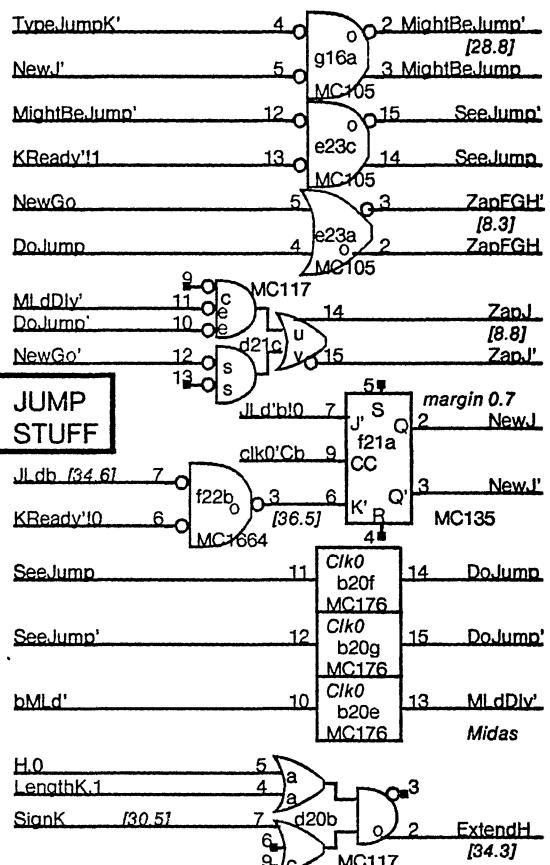
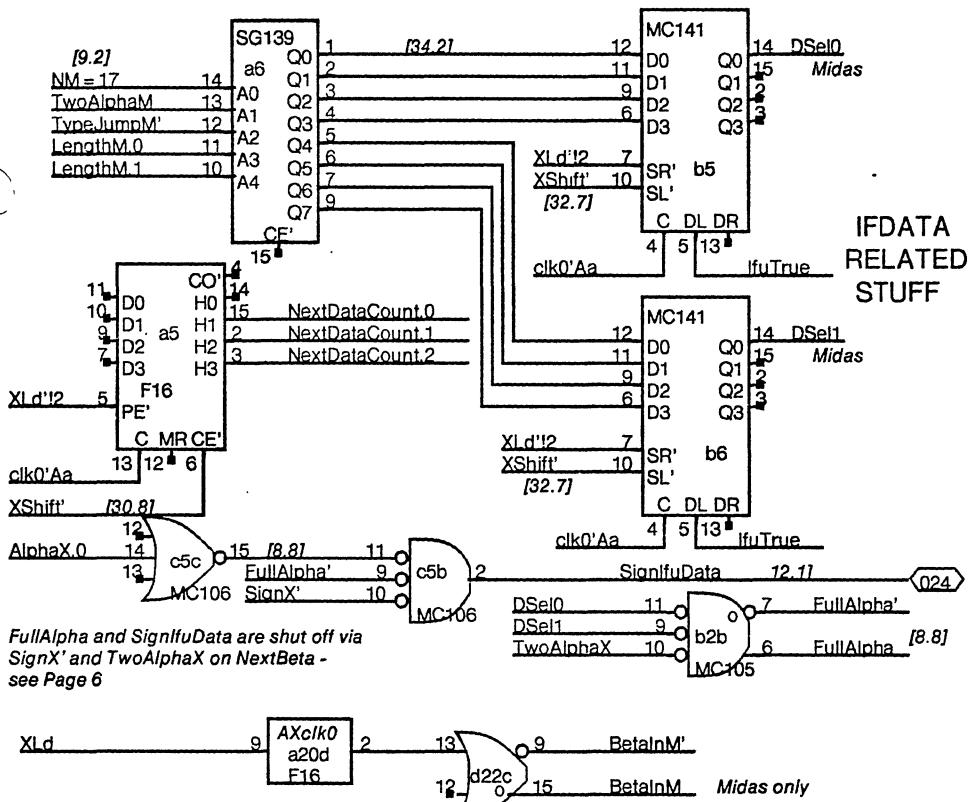
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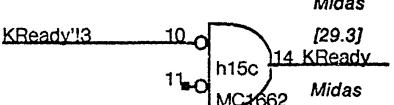
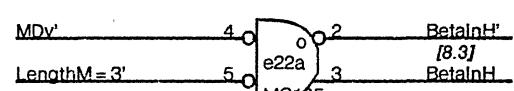
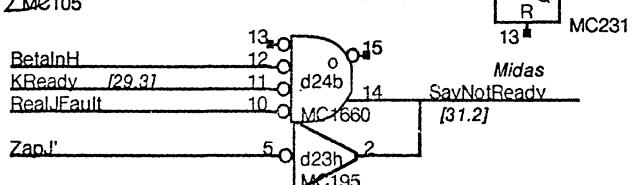
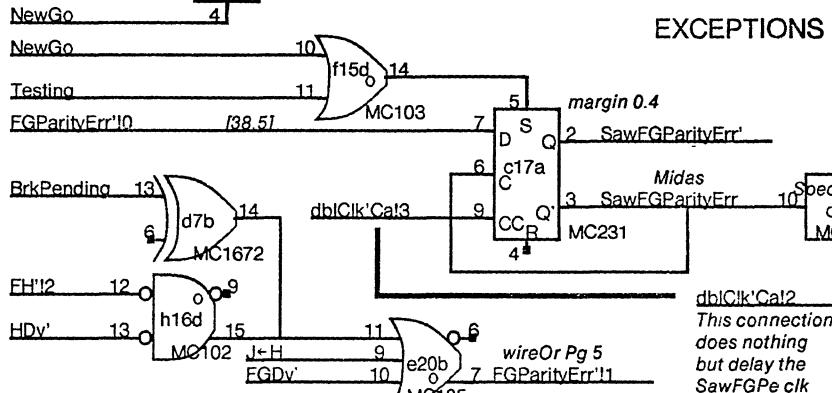
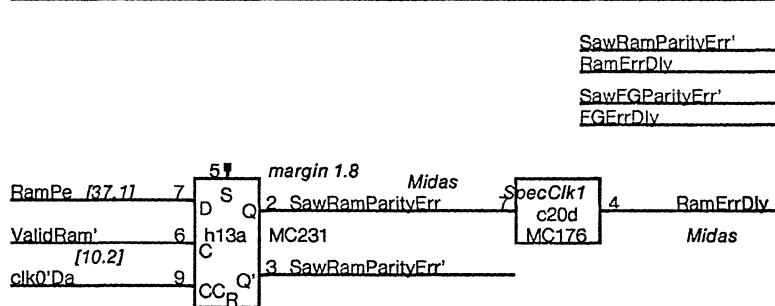


Combination of F valid and G invalid is impossible in First Half

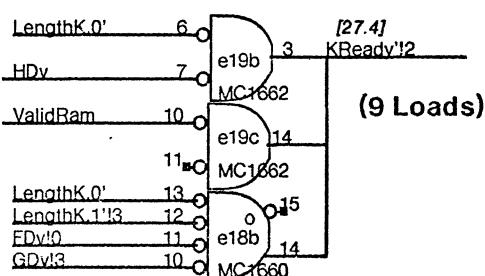


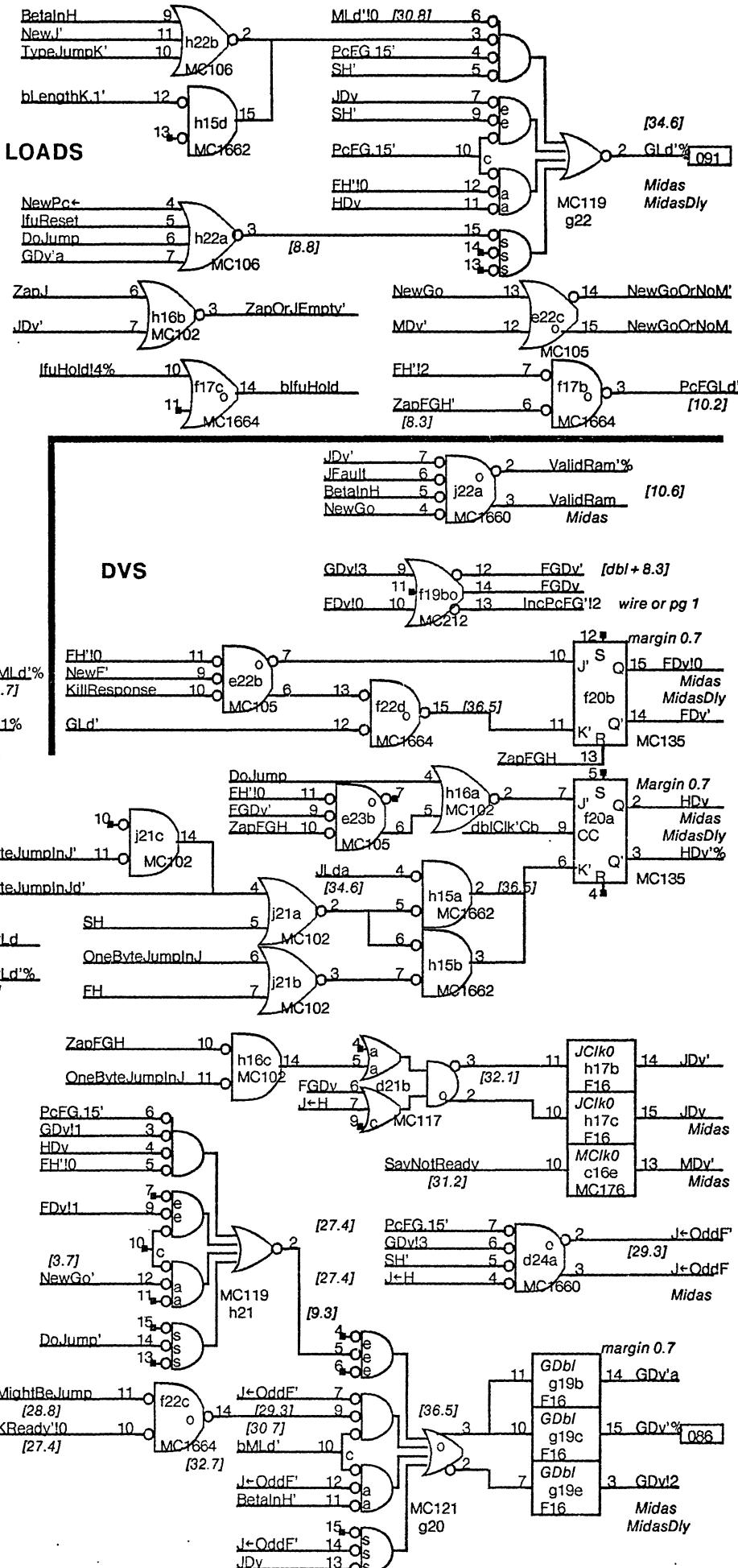
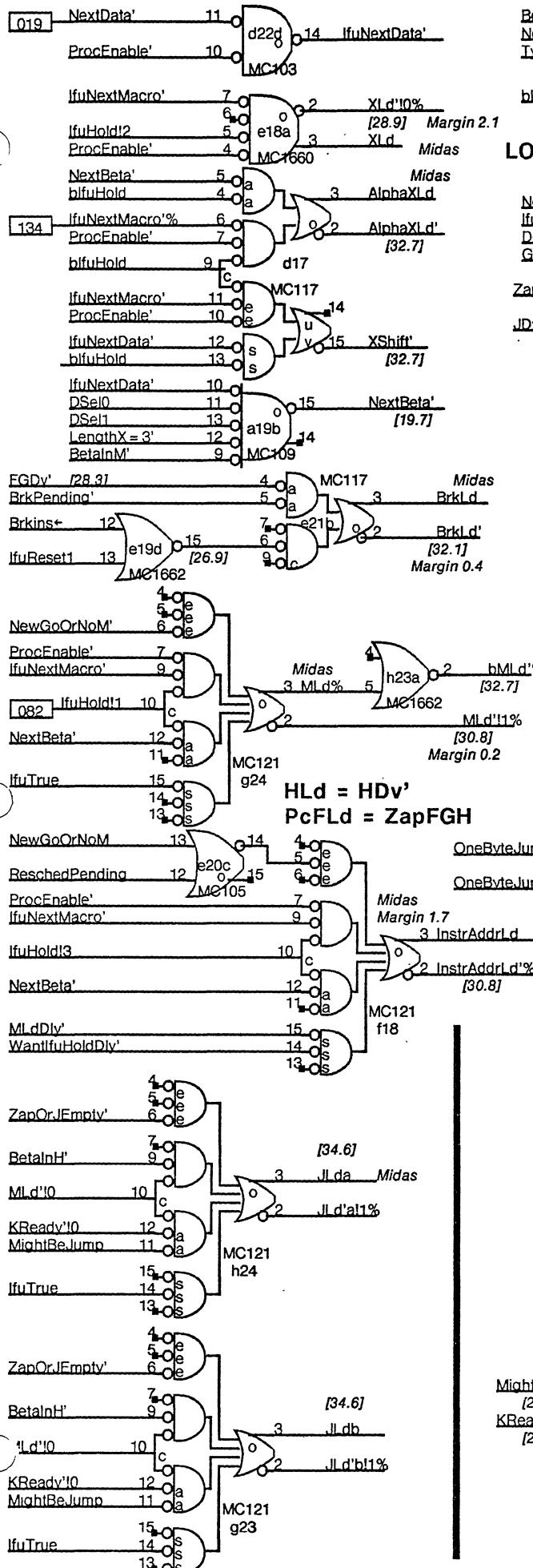


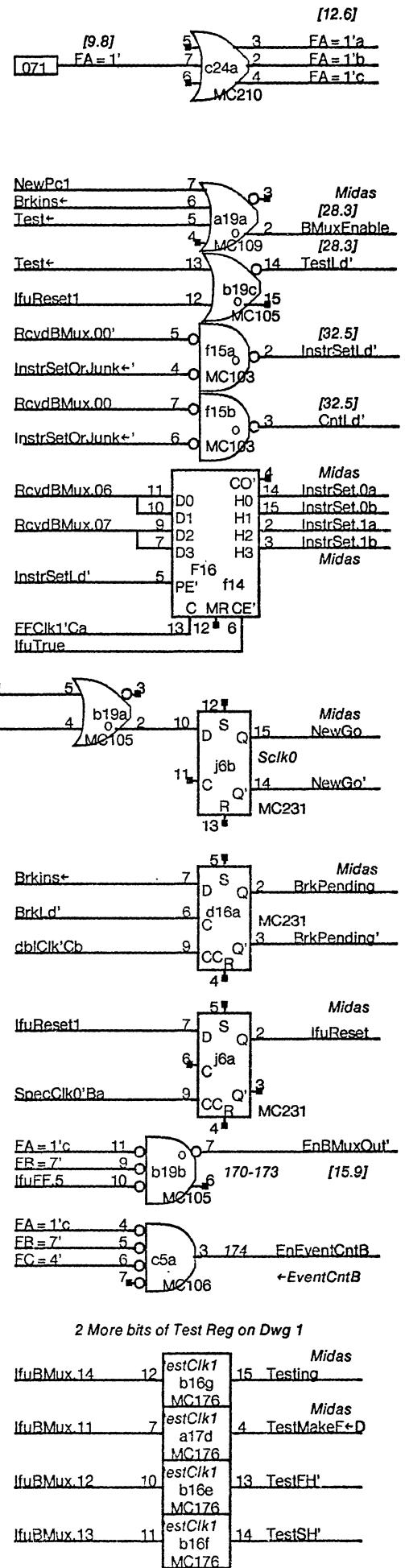
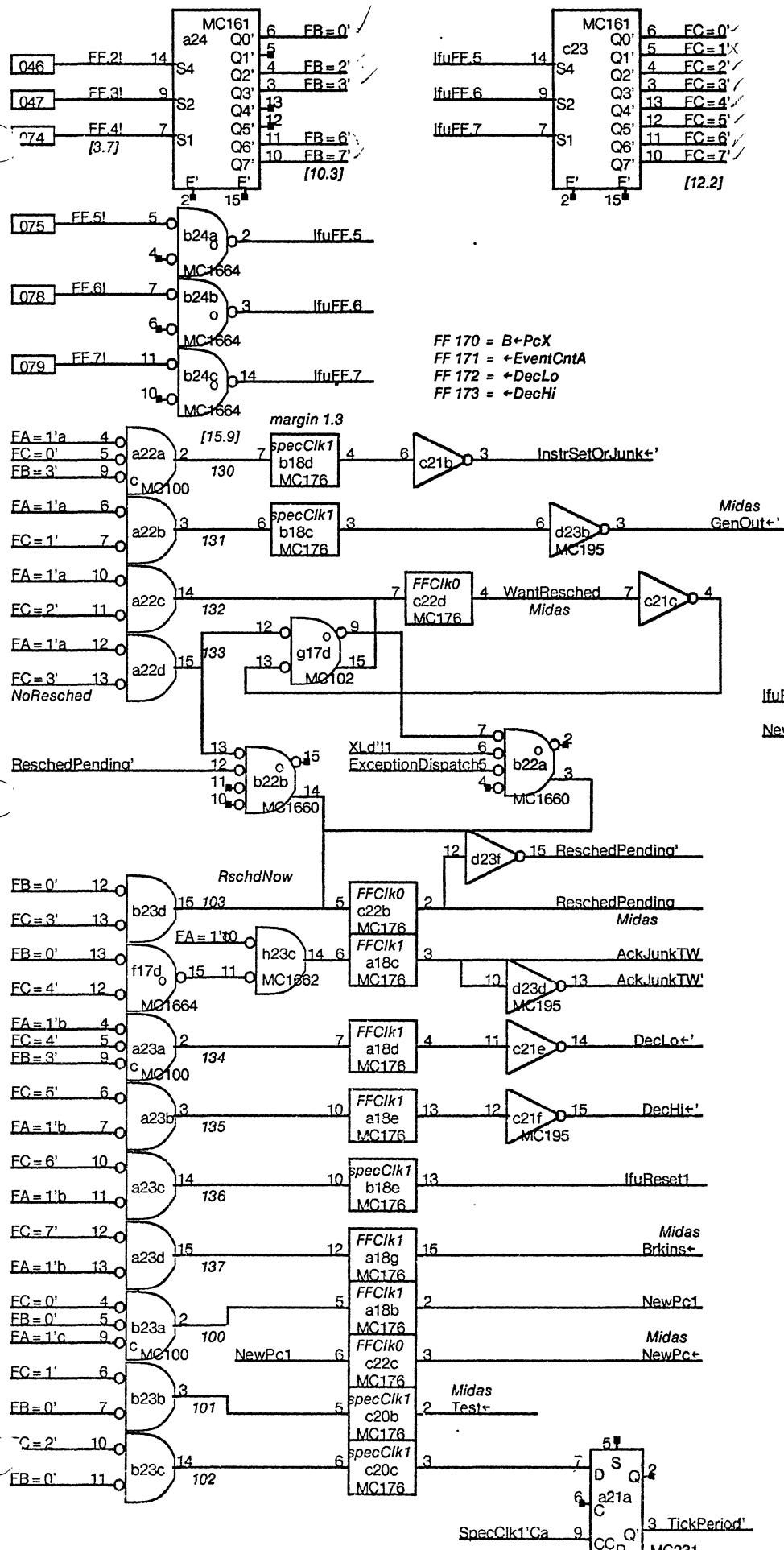
Wire Or Pg 3

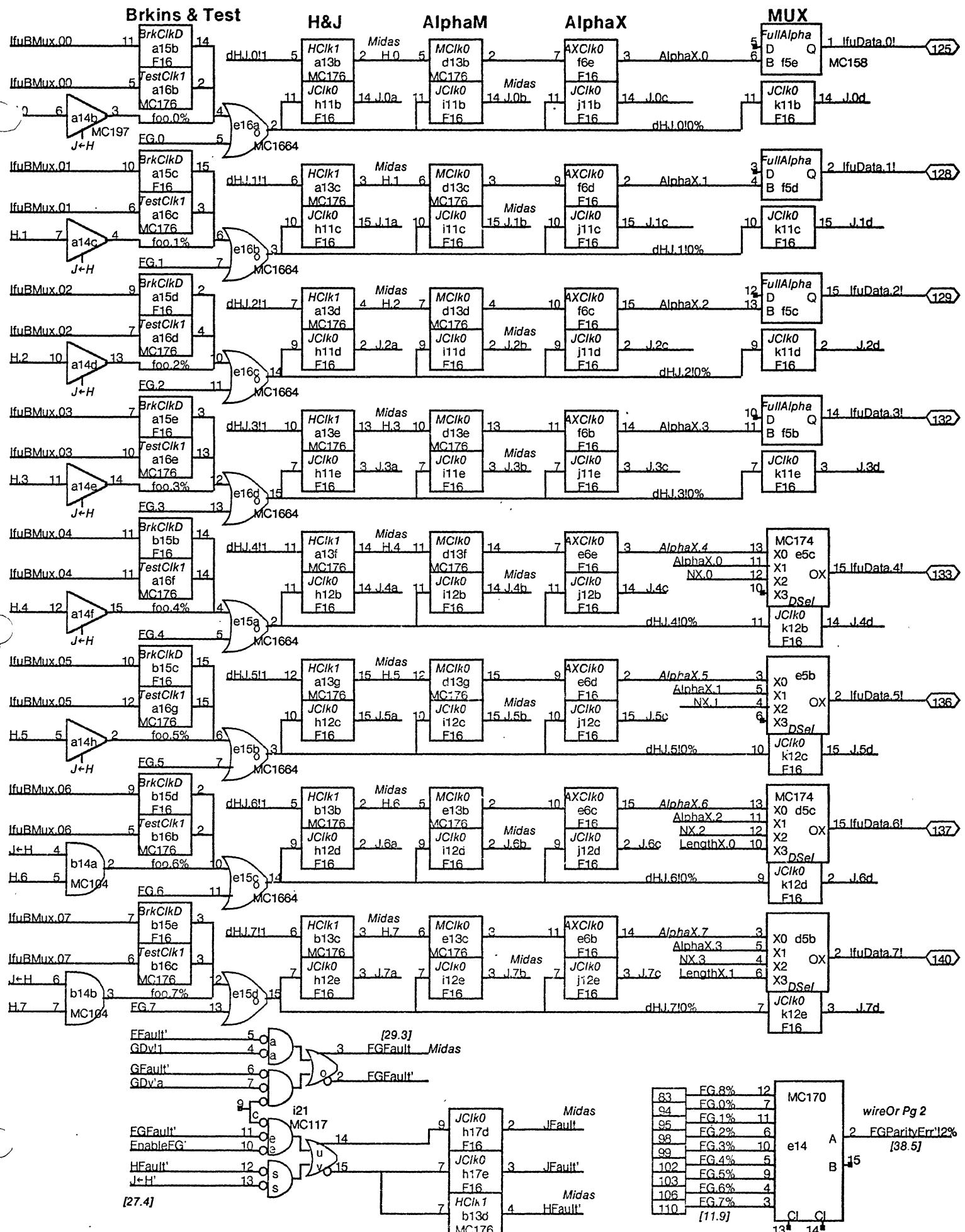


(9 Loads)





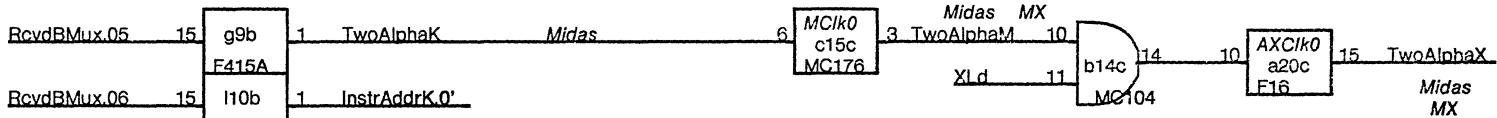
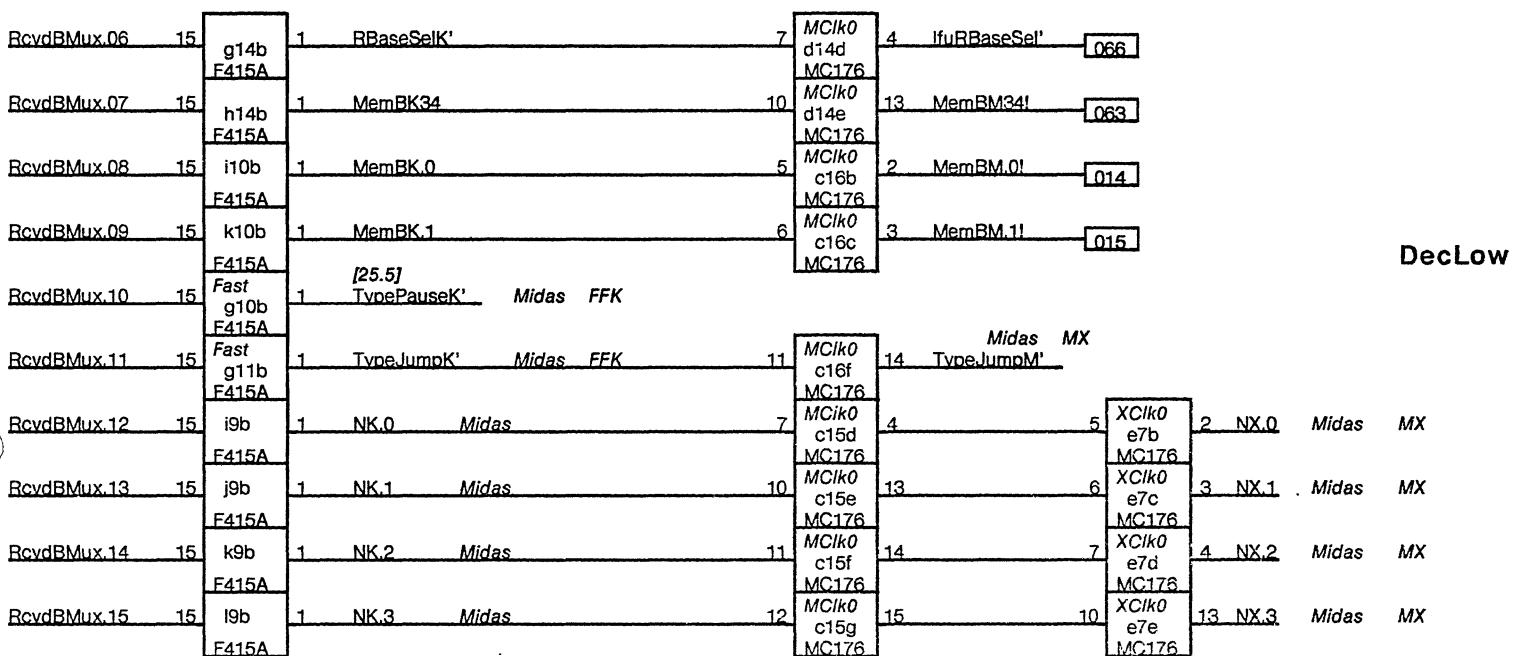
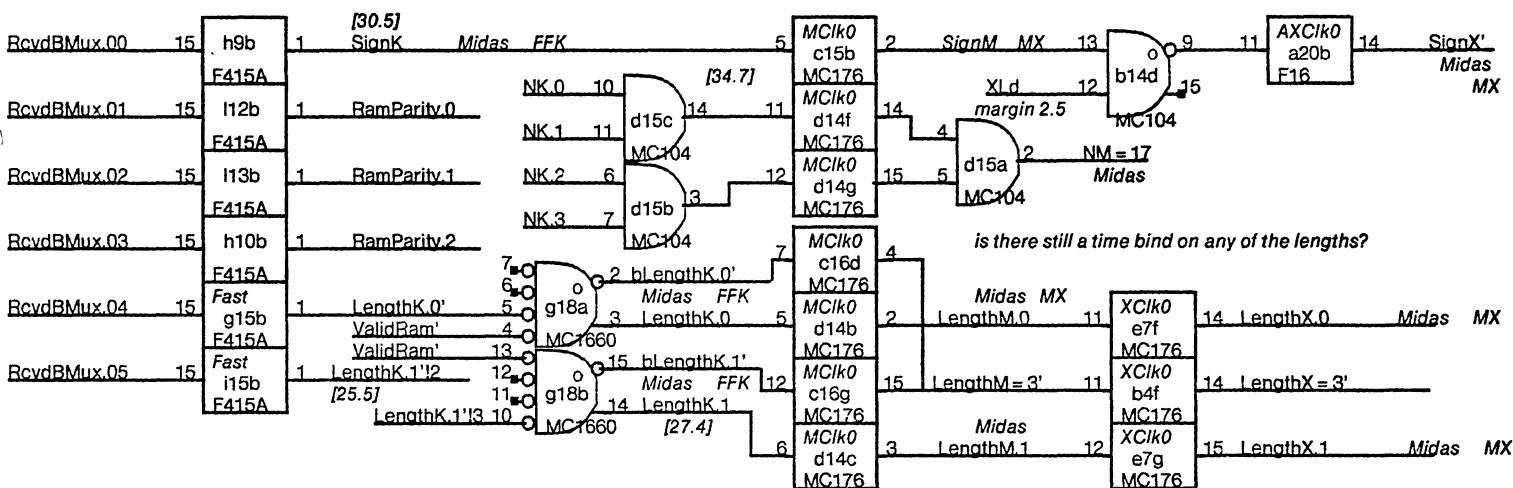




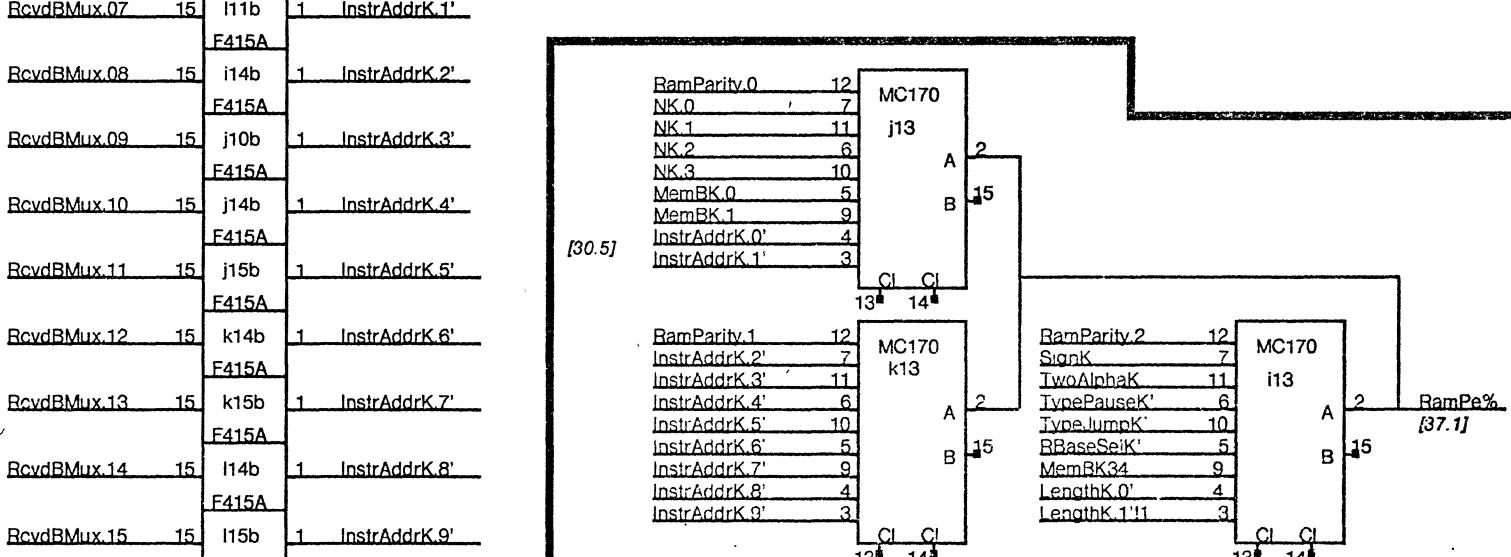
RAM

MREG

XREG

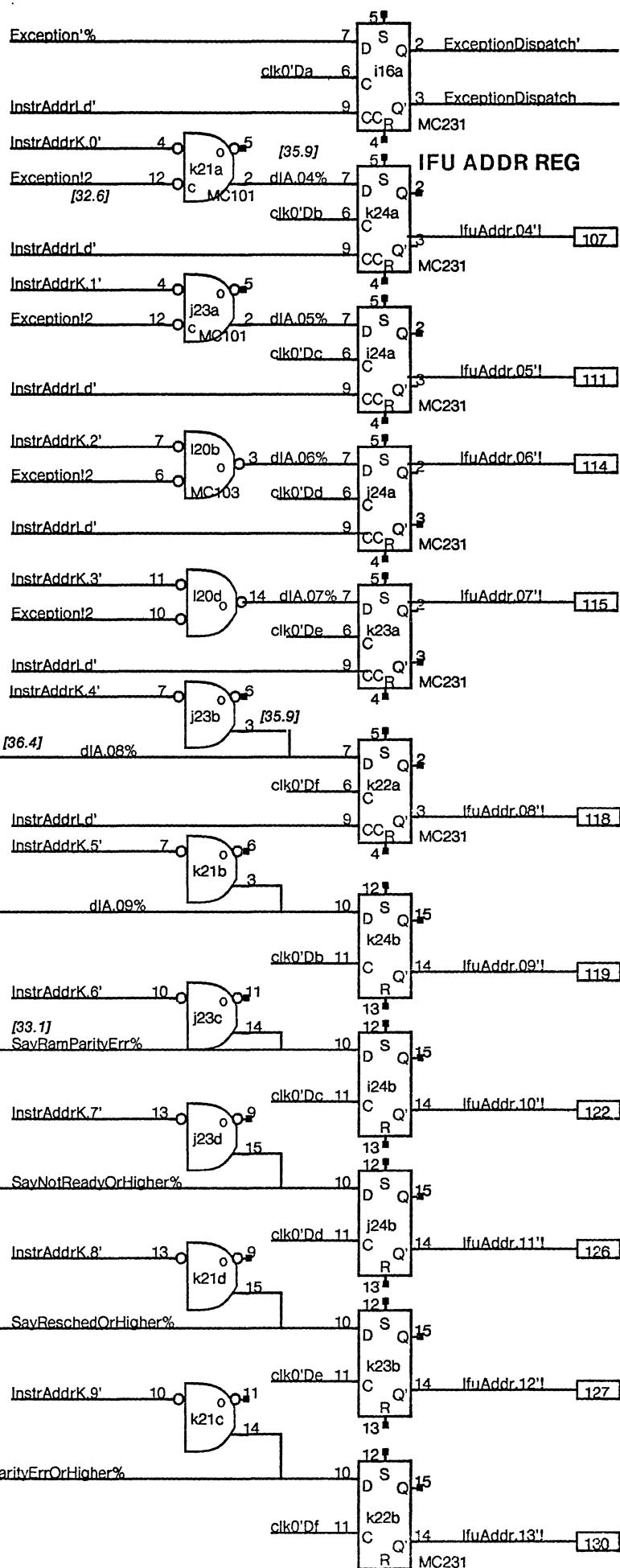
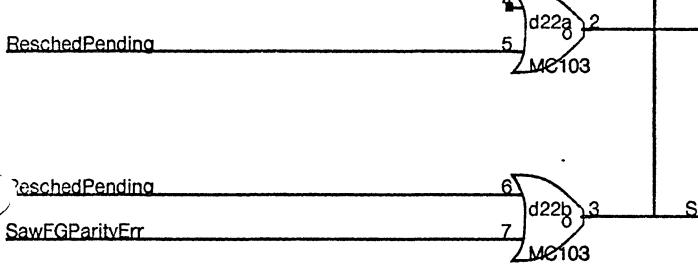
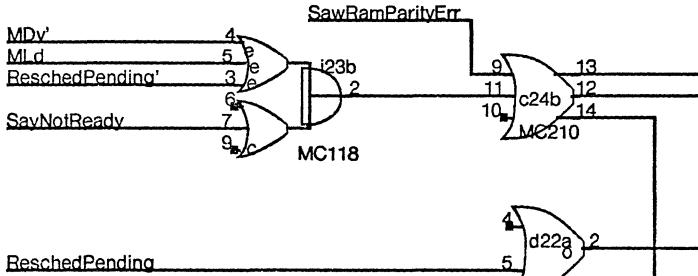
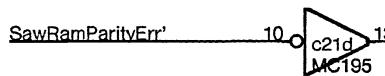
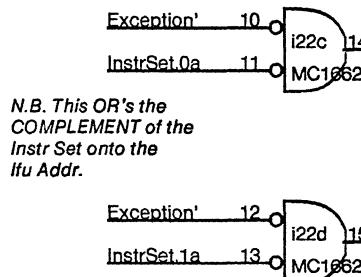
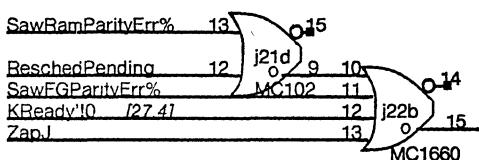
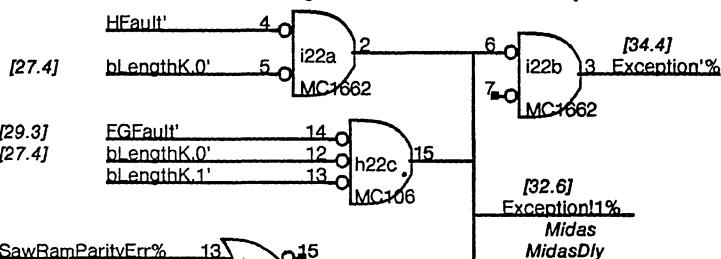


DecHi



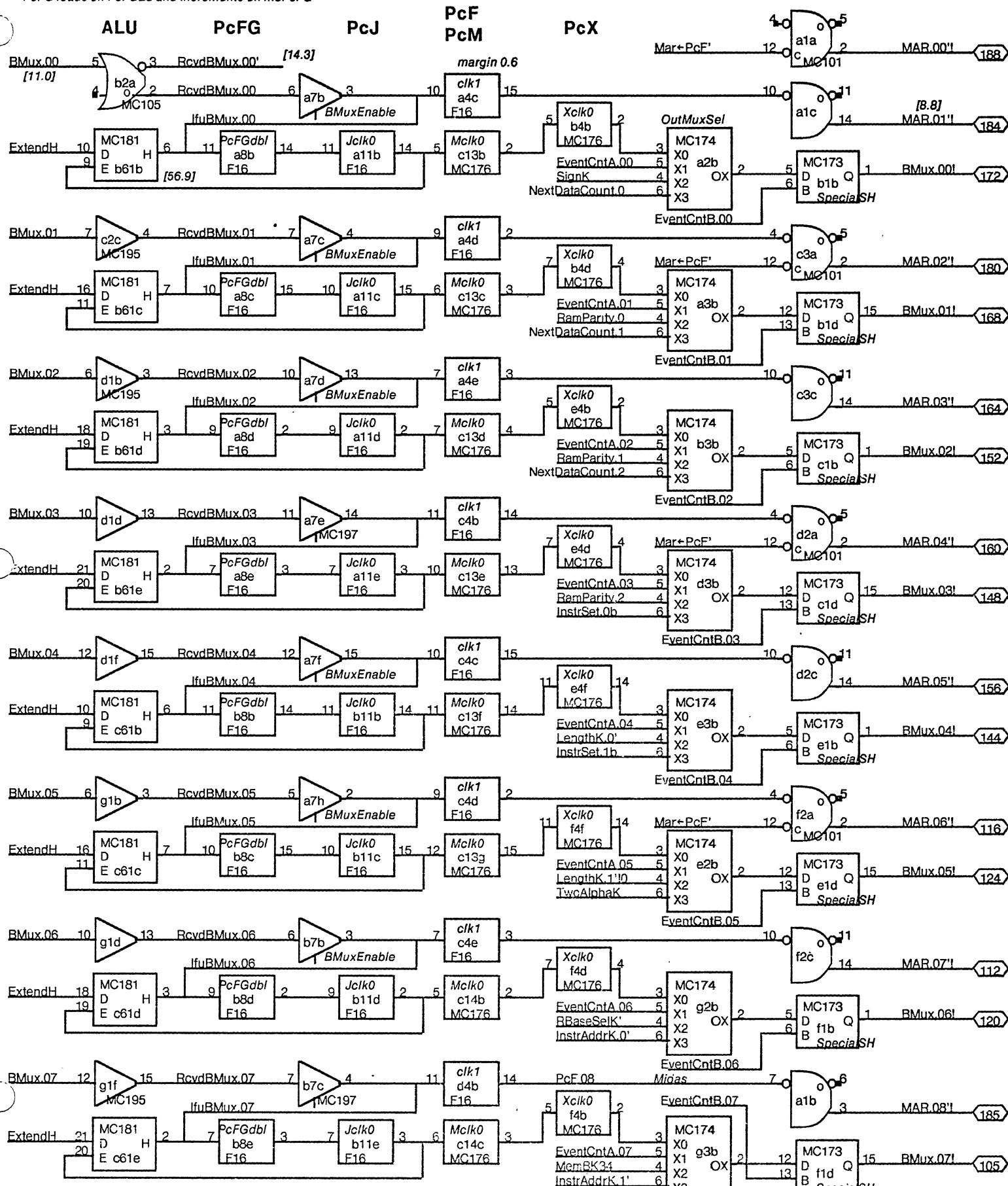
0	K Fault	low priority
4	FG Parity	
14	Resched	
34	Not Ready	
74	Ram Parity	high priority

KFault is JFault OR HFault&Length>1
OR FGFault&Length = 3



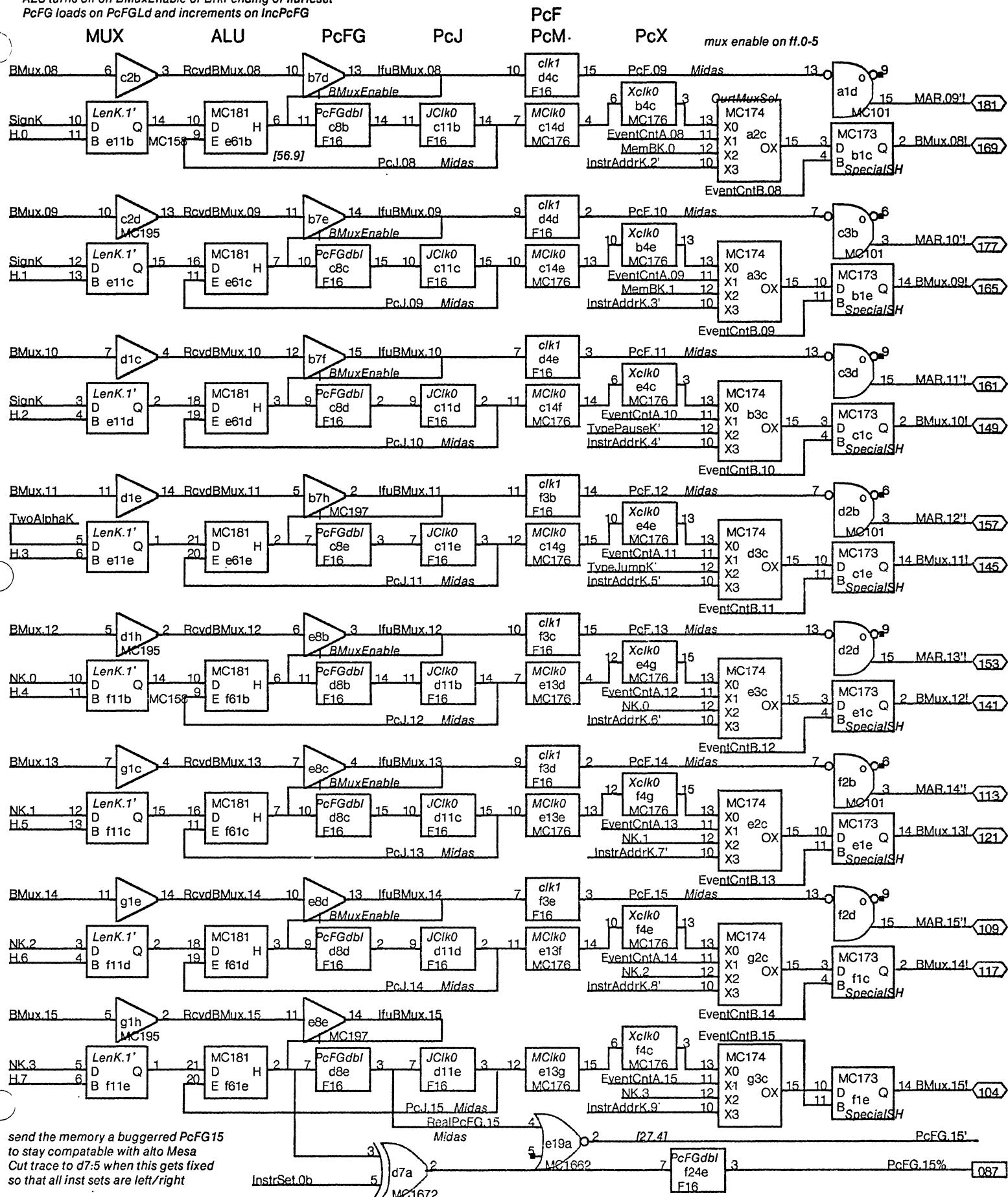
THE HIGH ORDER BYTE OF THE PC PIPE

PcJ loads on Jld And not J-H, increments on Jld
 PcF Loads on 'ZapFGH and increments on IncPcF
 ALU turns on BMuxEnable or BrkPending or IfuReset1
 PcFG loads on PcFGLd and increments on IncPcFG

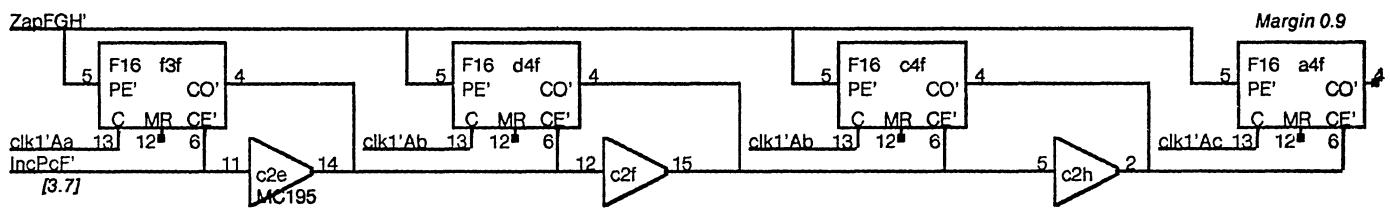


THE LOW ORDER BYTE OF THE PC PIPE

Pcj loads on Jld and not J+H, increments on Jld
 Pcf loads on ZapFGH and increments on IncPcf
 ALU turns off on BMuxEnable or BrkPending or IfuReset
 Pcfg loads on Pcfgld and increments on IncPcfg

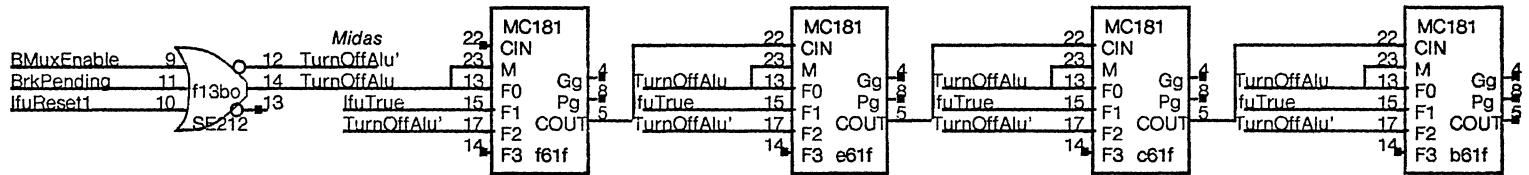


PcF Control



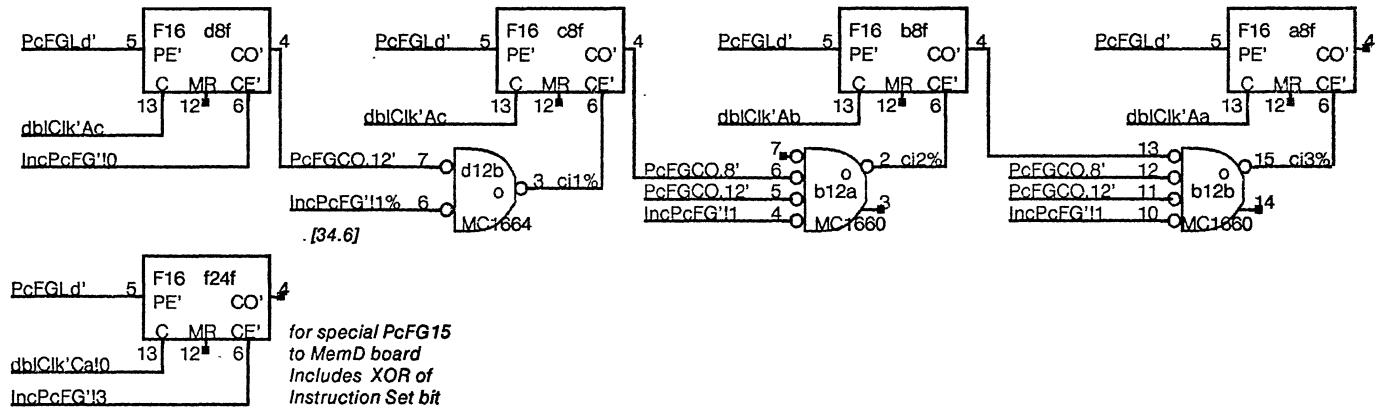
ALU Control

Low data in to high data out = 26.4



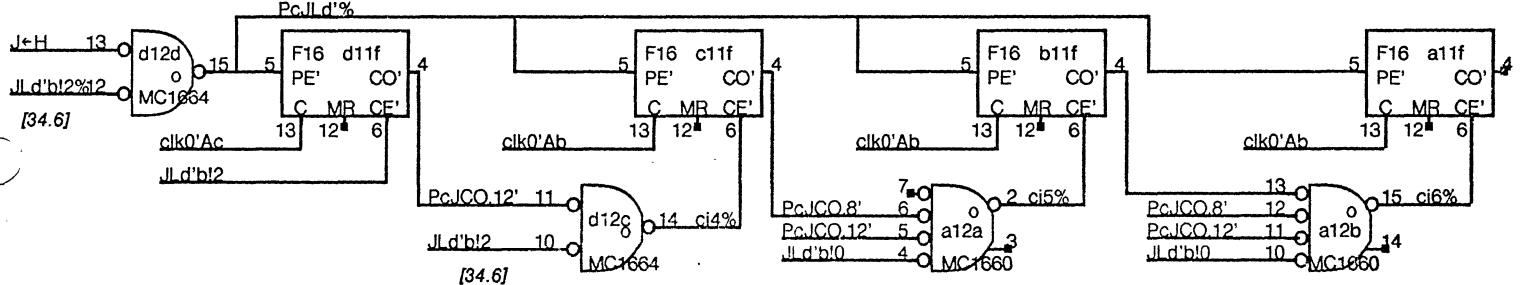
PcFG Control

[Margin 0.7 via Inc]

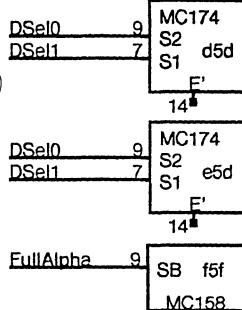


PcJ Control

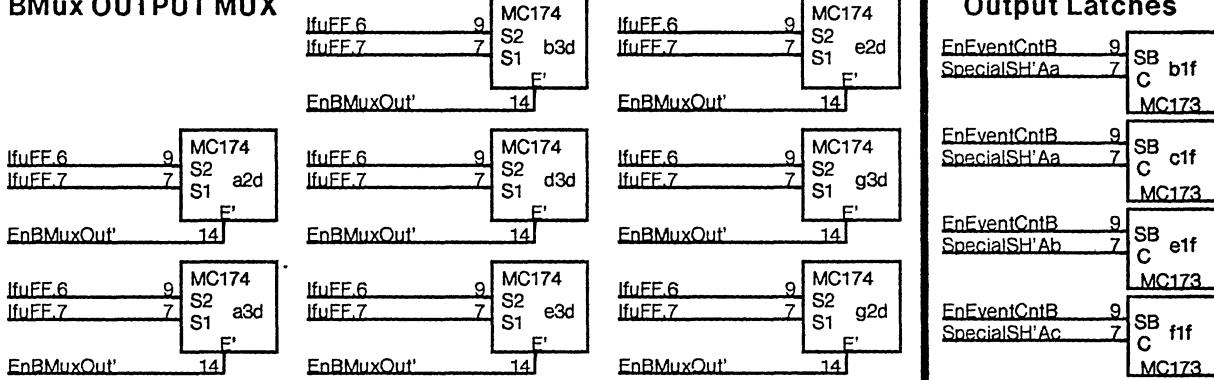
[Margin 0.7 via load and Inc]



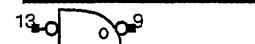
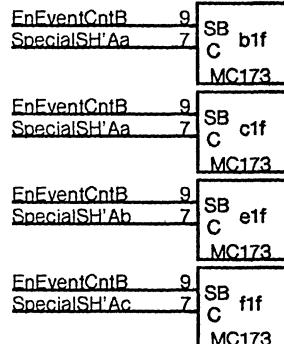
IfuData
OUTPUT MUX



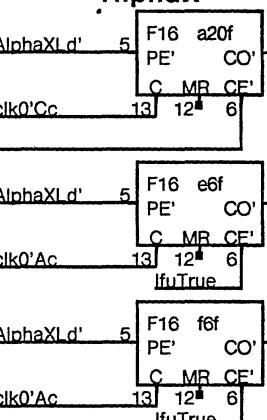
BMux OUTPUT MUX



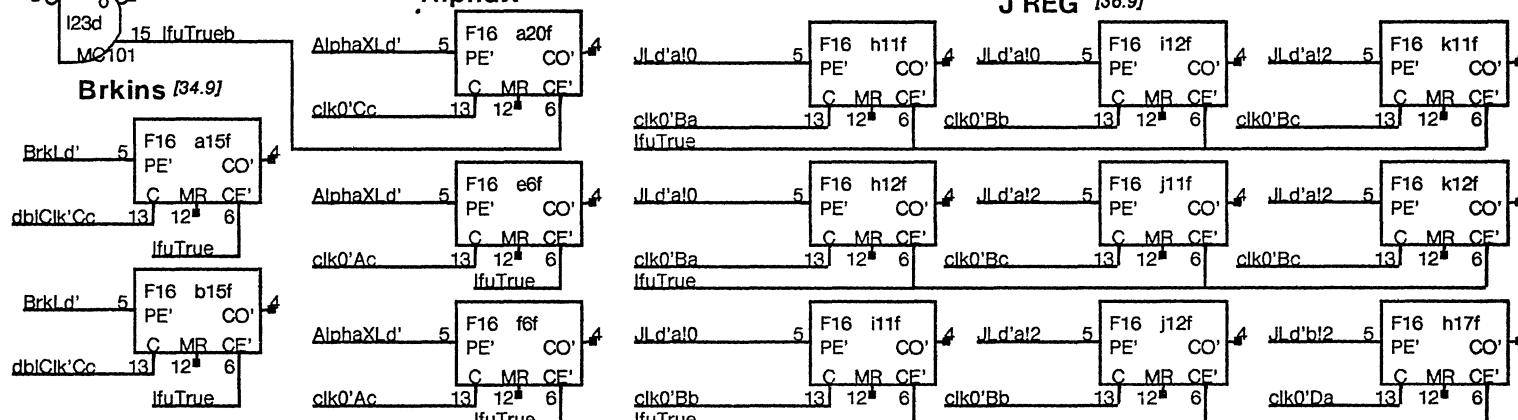
BMux
Output Latches



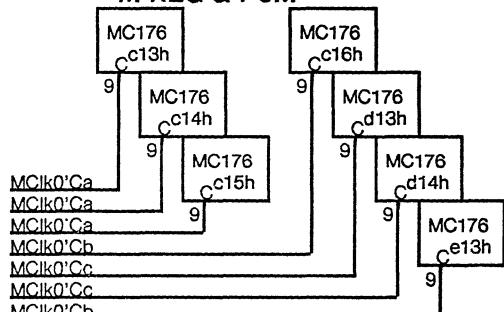
AlphaX [33.1]



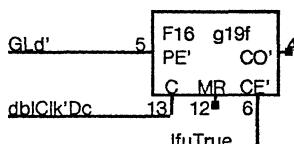
J REG [36.9]



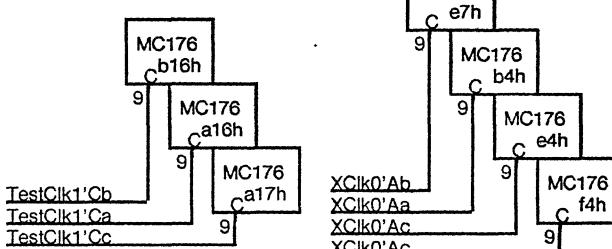
M REG & PcM [30.3]



GFAULT & GDV

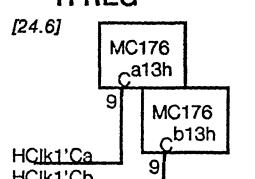


TEST REG

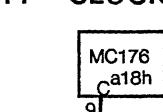


X REG and PcX [29.8]

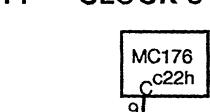
H REG



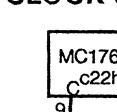
FF



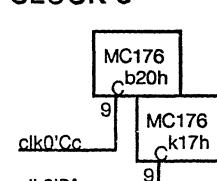
FF



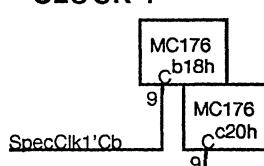
CLOCK 1



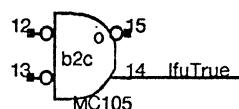
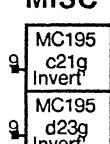
CLOCK 0



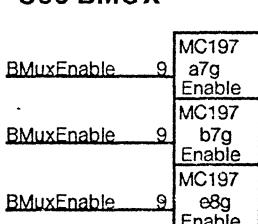
CLOCK 1 Without Test Mode



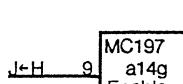
MISC



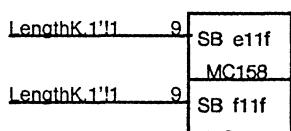
Use BMUX



J Loads from H



ALU INPUT MUX



low order bits must be fast!

TwoAlpha	
InstrSet.0a	2
	F415A
InstrSet.1a	3
J.0a	4
J.1a	5
J.2a	6
J.3a	7
J.4a	9
J.5a	10
J.6a	11
J.7a	12
	A3 g9c
	A4
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecHi←'	14 13

InstrAdd0	
InstrSet.0a	2
	F415A
InstrSet.1a	3
J.0a	4
J.1a	5
J.2a	6
J.3a	7
J.4a	9
J.5a	10
J.6a	11
J.7a	12
	A3 l10c
	A4
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecHi←'	14 13

1	
InstrSet.0a	2
	F415A
InstrSet.1a	3
J.0a	4
J.1a	5
J.2a	6
J.3a	7
J.4a	9
J.5a	10
J.6a	11
J.7a	12
	A3 l11c
	A4
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecHi←'	14 13

2	
InstrSet.0a	2
	F415A
InstrSet.1a	3
J.0a	4
J.1a	5
J.2a	6
J.3a	7
J.4a	9
J.5a	10
J.6a	11
J.7a	12
	A3 i14c
	A4
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecHi←'	14 13

3	
InstrSet.0a	2
	F415A
InstrSet.1a	3
J.0a	4
J.1a	5
J.2a	6
J.3a	7
J.4a	9
J.5a	10
J.6a	11
J.7a	12
	A4 j10c
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecHi←'	14 13

4	
InstrSet.0a	2
	F415A
InstrSet.1a	3
J.0c	4
J.1c	5
J.2c	6
J.3c	7
J.4c	9
J.5c	10
J.6c	11
J.7c	12
	A3 j14c
	A4
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecHi←'	14 13

5	
InstrSet.0a	2
	F415A
InstrSet.1a	3
J.0c	4
J.1c	5
J.2c	6
J.3c	7
J.4c	9
J.5c	10
J.6c	11
J.7c	12
	A4 j15c
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecHi←'	14 13

6	
InstrSet.0a	2
	F415A
InstrSet.1a	3
J.0c	4
J.1c	5
J.2c	6
J.3c	7
J.4c	9
J.5c	10
J.6c	11
J.7c	12
	A4 k14c
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecHi←'	14 13

7	
InstrSet.0a	2
	F415A
InstrSet.1a	3
J.0c	4
J.1c	5
J.2c	6
J.3c	7
J.4c	9
J.5c	10
J.6c	11
J.7c	12
	A4 k15c
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecHi←'	14 13

8	
InstrSet.0a	2
	F415A
InstrSet.1a	3
J.0c	4
J.1c	5
J.2c	6
J.3c	7
J.4c	9
J.5c	10
J.6c	11
J.7c	12
	A4 h14c
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecHi←'	14 13

InstrAdd1	
InstrSet.0a	2
	F415A
InstrSet.1a	3
J.0d	4
J.1d	5
J.2d	6
J.3d	7
J.4d	9
J.5d	10
J.6d	11
J.7d	12
	A3 l15c
	A4
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecHi←'	14 13

Sigh	
InstrSet.0a	2
	F415A
InstrSet.1a	3
J.0b	4
J.1b	5
J.2b	6
J.3b	7
J.4b	9
J.5b	10
J.6b	11
J.7b	12
	A4 h9c
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecLo←'	14 13

Ram P50	
InstrSet.0a	2
	F415A
InstrSet.1a	3
J.0d	4
J.1d	5
J.2d	6
J.3d	7
J.4d	9
J.5d	10
J.6d	11
J.7d	12
	A4 l12c
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecLo←'	14 13

Ram P51	
InstrSet.0a	2
	F415A
InstrSet.1a	3
J.0d	4
J.1d	5
J.2d	6
J.3d	7
J.4d	9
J.5d	10
J.6d	11
J.7d	12
	A4 l13c
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecLo←'	14 13

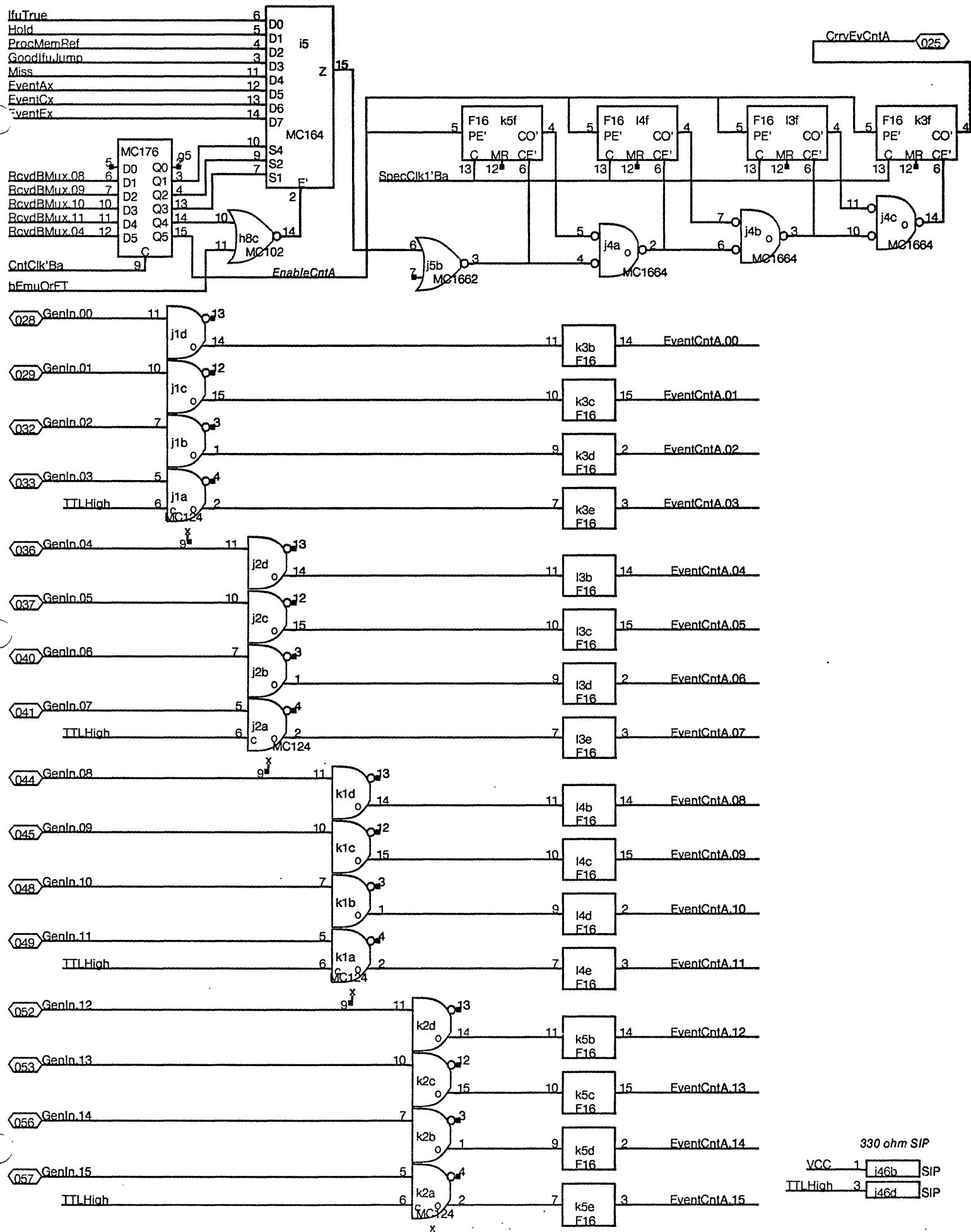
Ram P52	
InstrSet.0b	2
	F415A
InstrSet.1b	3
J.0b	4
J.1b	5
J.2b	6
J.3b	7
J.4b	9
J.5b	10
J.6b	11
J.7b	12
	A3 k9c
	A4
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecLo←'	14 13

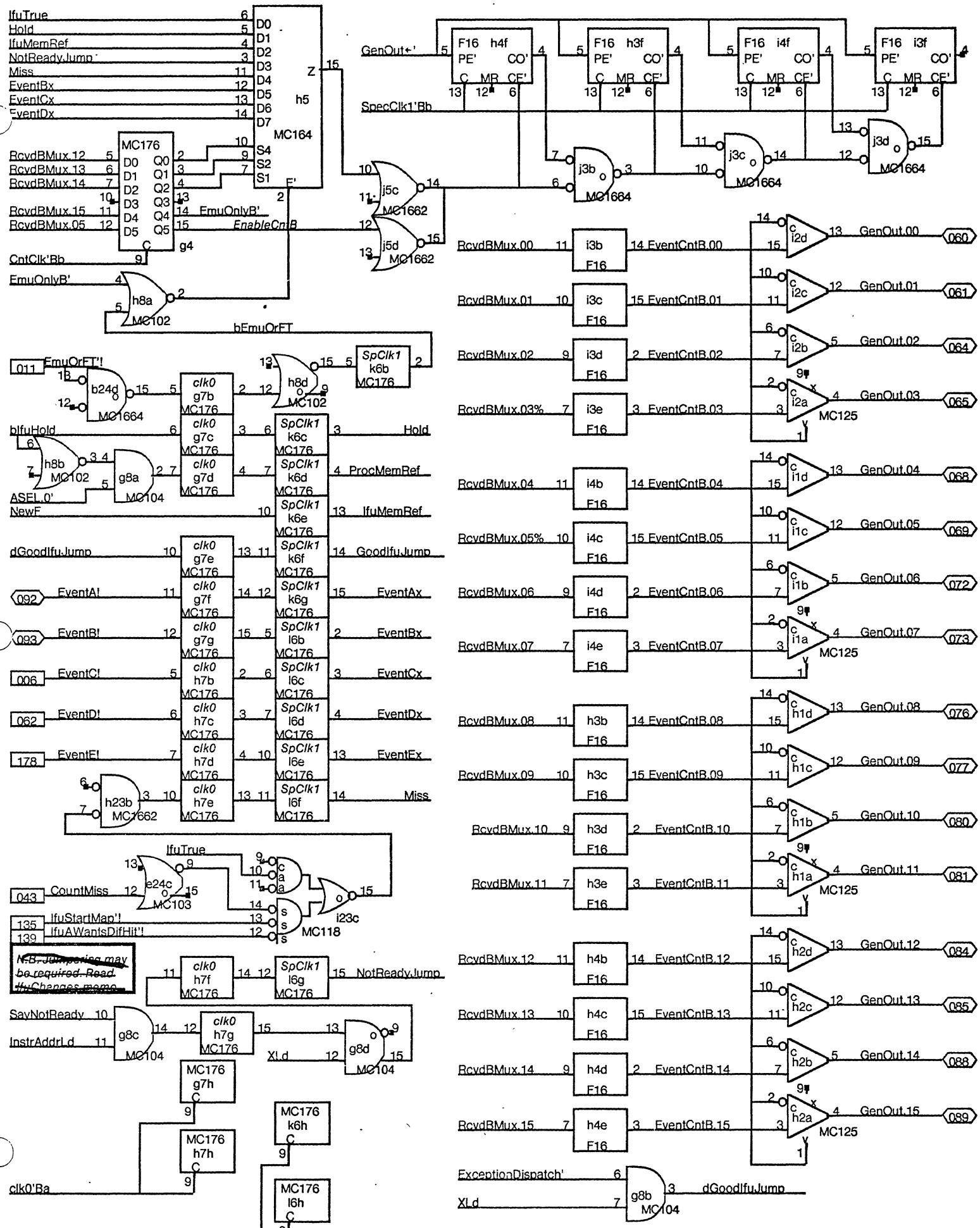
A3	
InstrSet.0b	2
	F415A
InstrSet.1b	3
J.0a	4
J.1a	5
J.2a	6
J.3a	7
J.4a	9
J.5a	10
J.6a	11
J.7a	12
	A3 g9c
	A4
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecLo←'	14 13

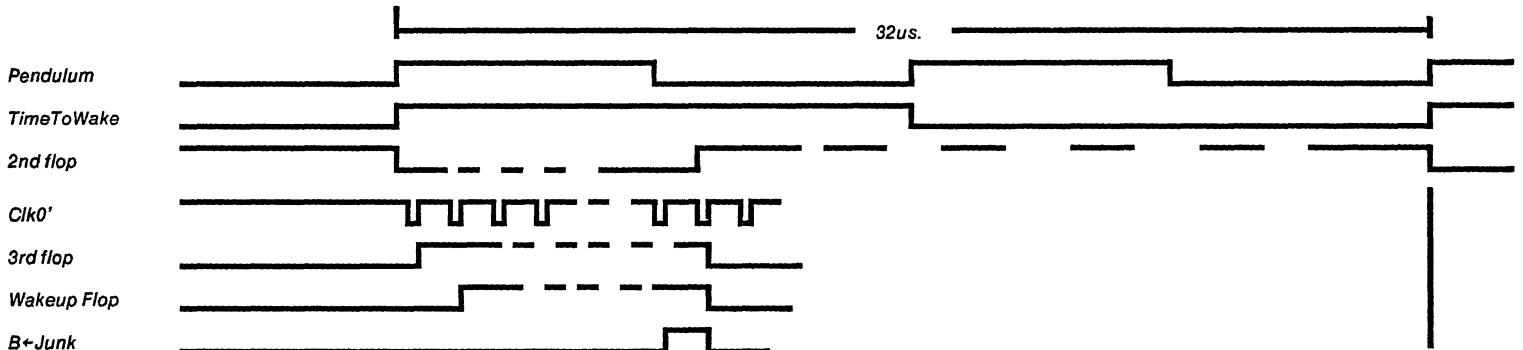
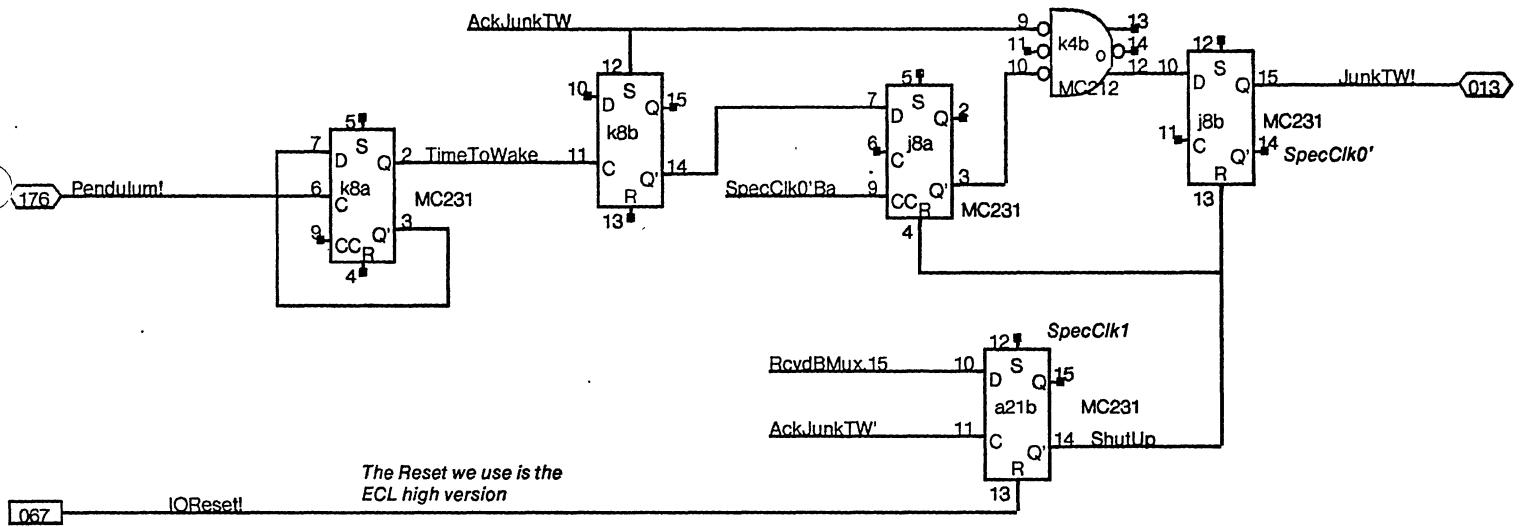
TypePause	
InstrSet.0b	2
	F415A
InstrSet.1b	3
J.0a	4
J.1a	5
J.2a	6
J.3a	7
J.4a	9
J.5a	10
J.6a	11
J.7a	12
	A4 g10c
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecLo←'	14 13

TypeJump	
InstrSet.0b	2
	F415A
InstrSet.1b	3
J.0a	4
J.1a	5
J.2a	6
J.3a	7
J.4a	9
J.5a	10
J.6a	11
J.7a	12
	A4 g11c
	A5
	A6
	A7
	A8
	A9
	CE' WF'
DecLo←'	14 13

FBaseSel	
InstrSet.0b	2
	F415A
InstrSet.1b	3
J.0a	4
J.1a	5
J.2a	6
J.3a	7
J.4a	9
J.5a	10
J.6a	11
J.7a	12

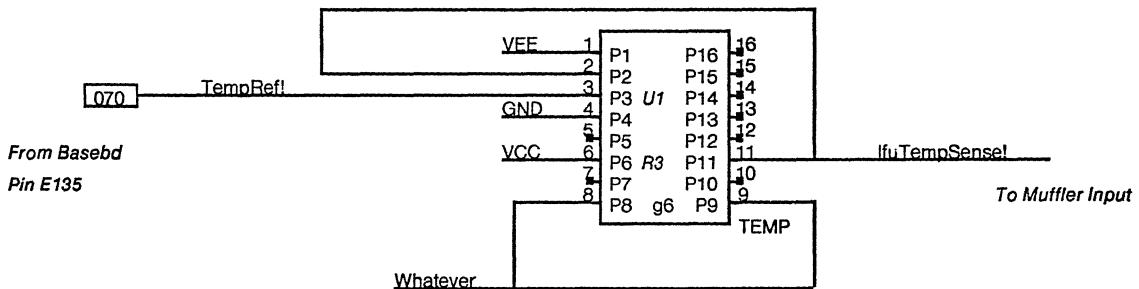






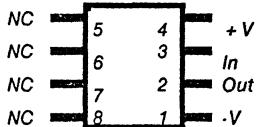
Do it again here

Temperature Sensor

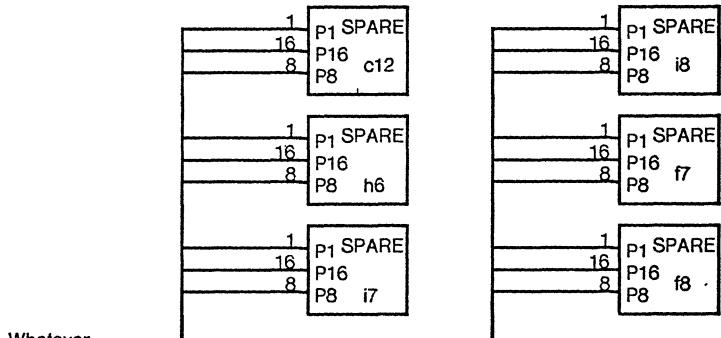


U1 = LM3911

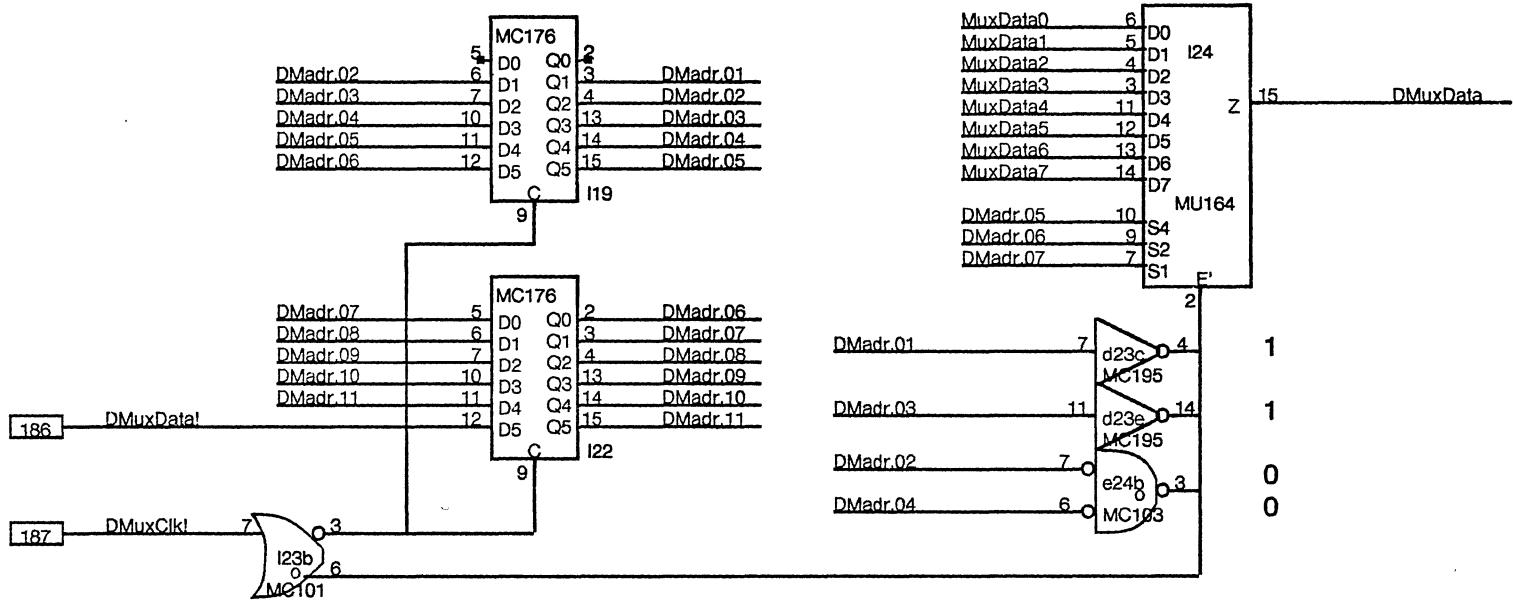
$$R3 = 20K$$



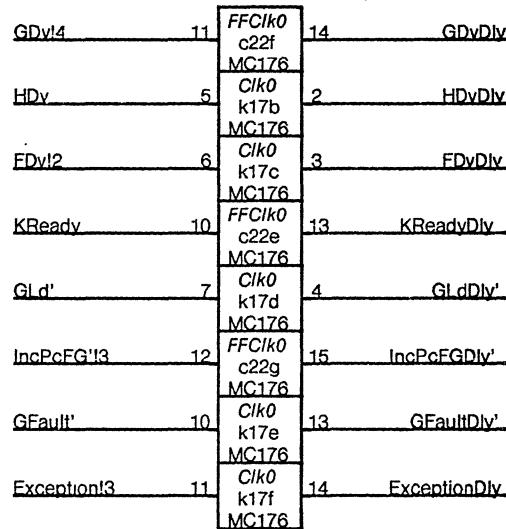
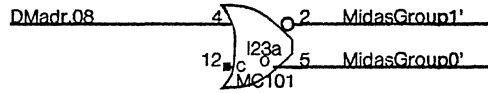
LM3911
(ECL)

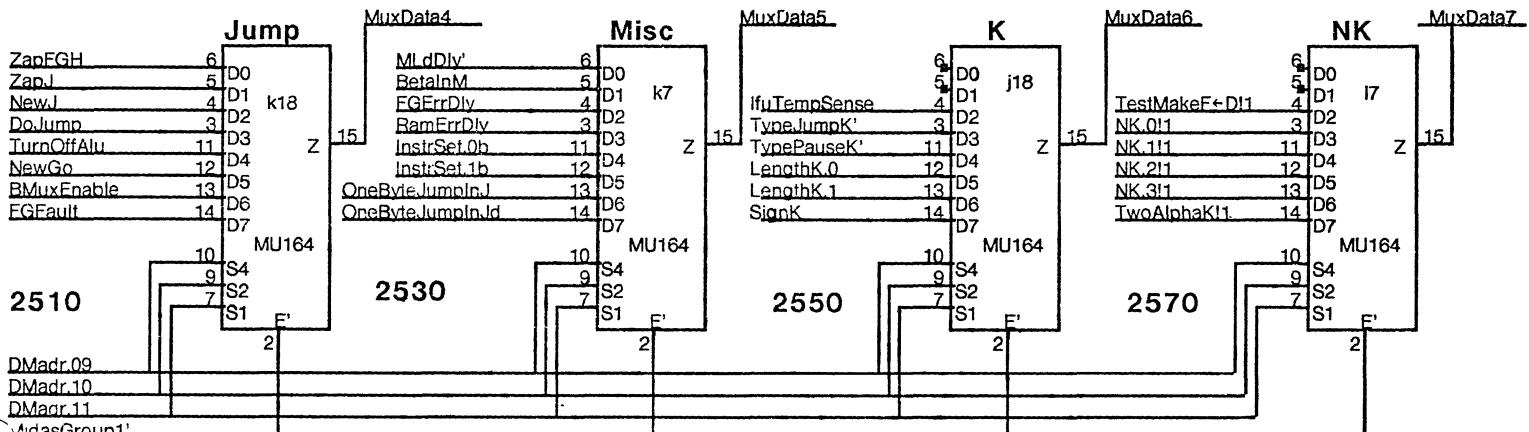
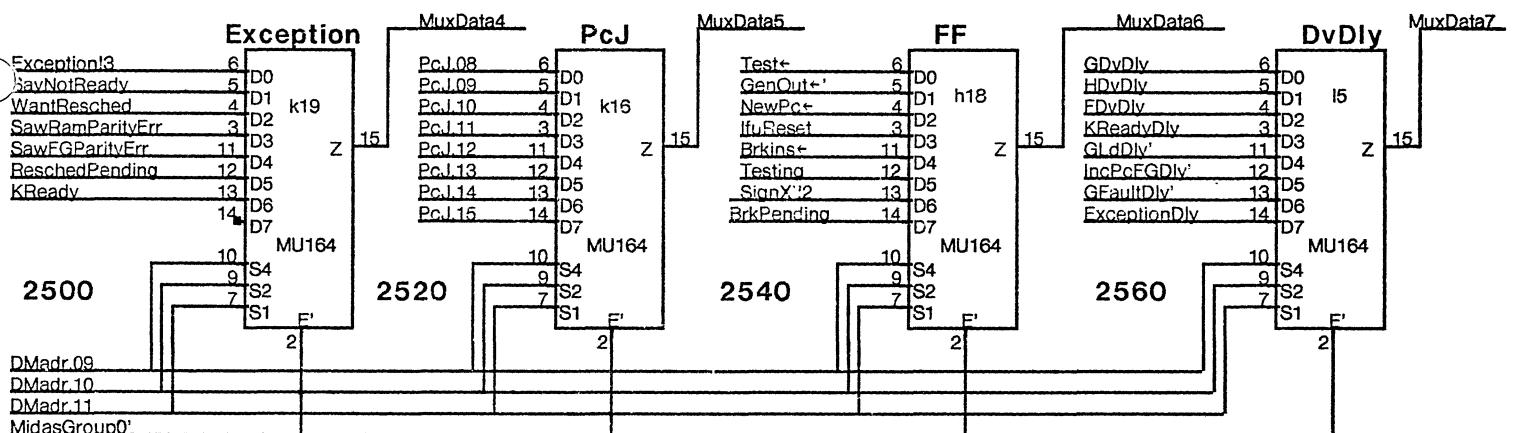
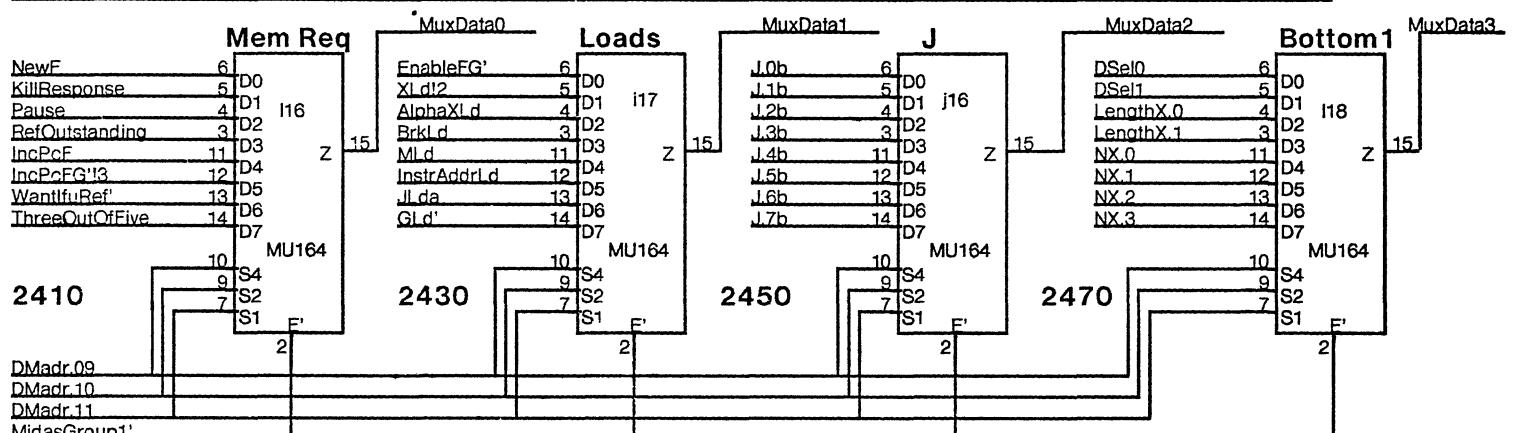
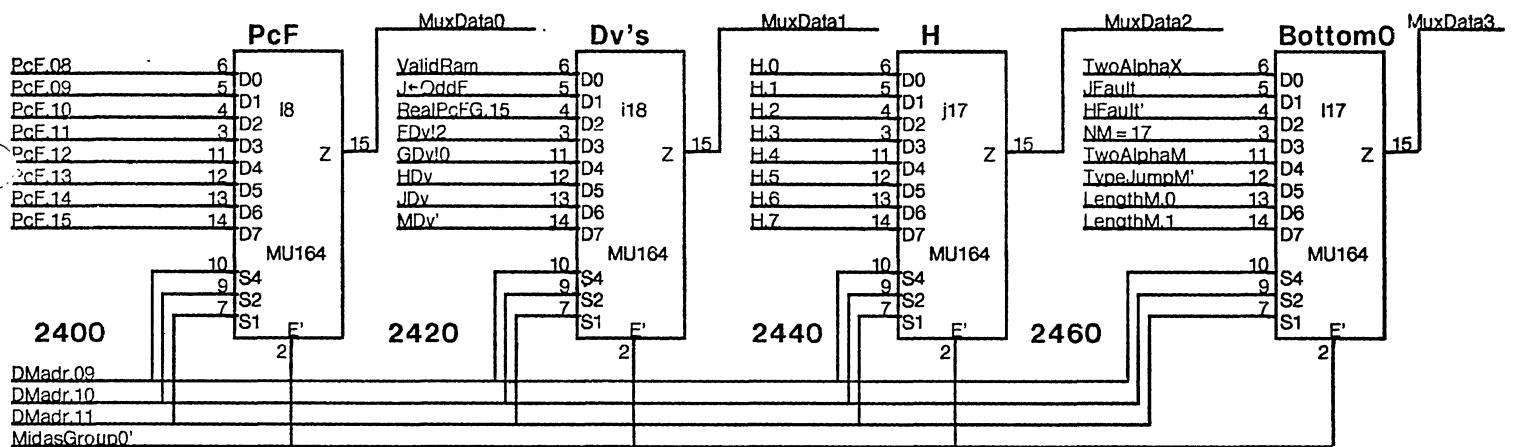


Muffler Control

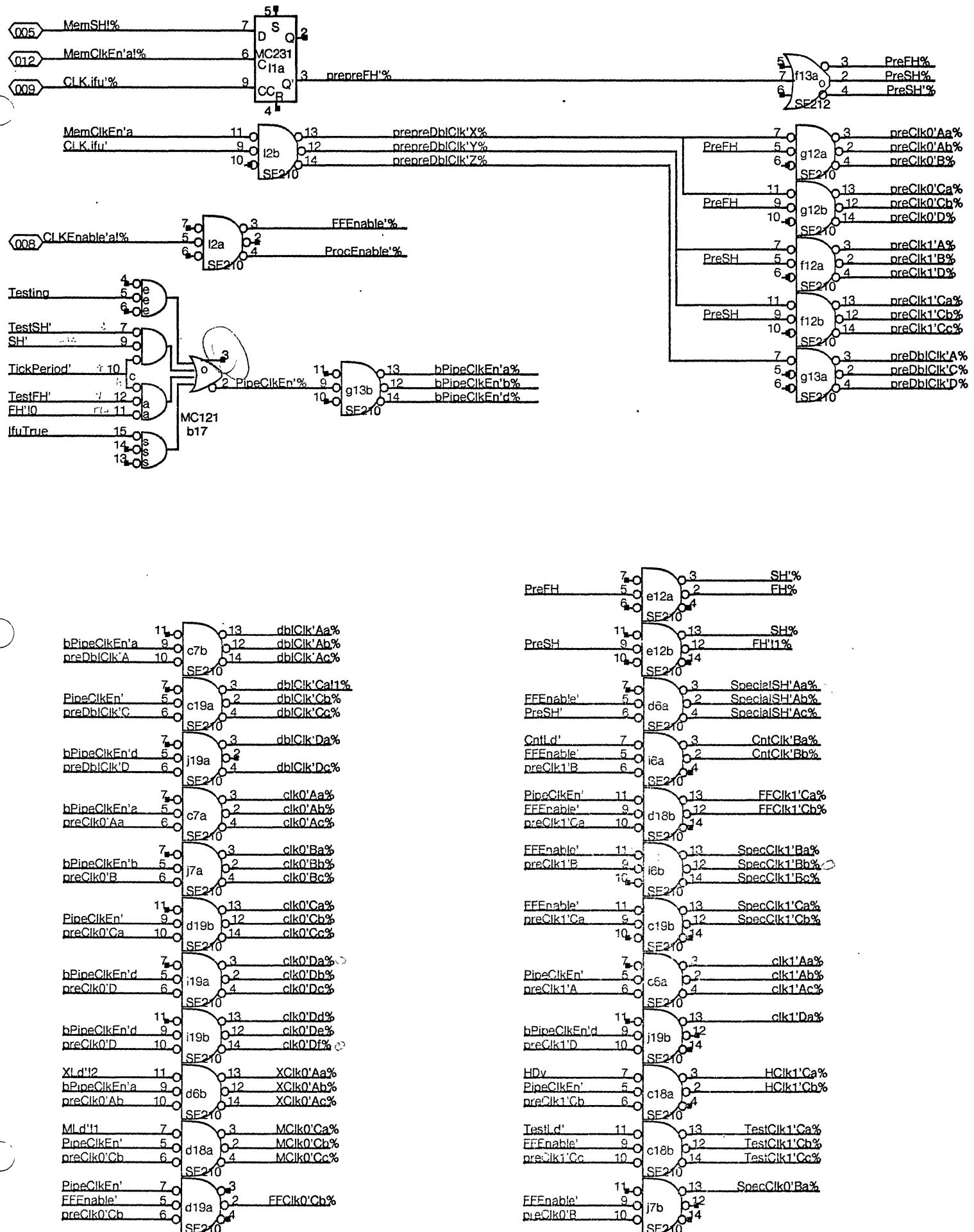


We respond to 2400 thru 2577
Tho we are allocated to 2777.





Word0: MemRQ
 Word1: Loads
 Word2: HJ
 Word3: MX
 Word4: JmpExc
 Word5: PcJ
 Word6: FFK
 Word7: DvNK



MAR 0,8,1,9,2,10

GenIn (28-57)

GenOut (60-89)

BMux 0,8,1,9 MAR 3,11,4,12,5,13 BMux 2,10,3,11,4,12

IfuData

BMux 5,13,6,14

BMux 7,15

01	A MAR 00 b MAR 08 c MAR 01 d MAR 09	b BMux 00 SS c BMux 08 d BMux 01 e BMux 09	101	173	b BMux 02 SS c BMux 10 d BMux 03 e BMux 11	173	b RcvdBMux 02 c RcvdBMux 10 d RcvdBMux 03 e RcvdBMux 11 f RcvdBMux 04 h RcvdBMux 12	195	b BMux 04 SS c BMux 12 d BMux 05 e BMux 13	b BMux 06 SS c BMux 14 d BMux 07 e BMux 15	173	173	
	b dBmux 00 c dBmux 08	a RcvdBMux 00 B FullAlpha c IfuTrue	174	105	b RcvdBMux 08 c RcvdBMux 01 d RcvdBMux 09 e PcfCarry f PcfCarry h PcfCarry	195	A MAR 04 b MAR 12 c MAR 05 d MAR 13	101	b dBmux 05 c dBmux 13	A MAR 06 b MAR 14 c MAR 07 d MAR 15	174	101	
03	b dBmux 01 c dBmux 09	b dBmux 02 c dBmux 10	174	174	A MAR 02 b MAR 10 c MAR 03 d MAR 11	101	b dBmux 03 c dBmux 11	174	b dBmux 04 c dBmux 12	b Pcf 12 c Pcf 13 d Pcf 14 e Pcf 15	174	F16	
	b Pcf 01 C1 c Pcf 02 d Pcf 03	b Pcf 00 X0 c Pcf 08 d Pcf 01 e Pcf 09 f LengthX=3' g	F16	176	b Pcf 04 C1 c Pcf 05 d Pcf 06 e Pcf 07	F16	b Pcf 08 C1 c Pcf 09 d Pcf 10 e Pcf 11	F16	b Pcf 02 X0 c Pcf 10 d Pcf 03 e Pcf 11 f Pcf 04 g Pcf 12	b Pcf 07 X0 c Pcf 15 d Pcf 06 e Pcf 14 f Pcf 05 g Pcf 13	176	176	
05	b NextData 0 C0 c NextData 1 d NextData 2	DSel0 C0	F16	141	A EnEventCntB b SignifData c AlphaX'	106	b IfuData 7 c IfuData 6	174	b IfuData 5 c IfuData 4	b IfuData 3 c IfuData 2 d IfuData 1 e IfuData 0	174	158	
	DSelProm	DSel1 C0	139	141	a clk1' A b	210	a SpecSH A b XClk0 A	210	a AlphaX 07 C0 b AlphaX 06 d AlphaX 05 e AlphaX 04	b AlphaX 03 C0 c AlphaX 02 d AlphaX 01 e AlphaX 00	F16	F16	
07	b IfuBmux 00 c IfuBmux 01 d IfuBmux 02 e IfuBmux 03 f IfuBmux 04 h IfuBmux 05	b IfuBmux 06 c IfuBmux 07 d IfuBmux 08 e IfuBmux 09 f IfuBmux 10 h IfuBmux 11	197	197	a clk0' A b dblclk A	210	a PcfG.15 b dSaw FGPE c	1672	b NX.0 X0 c NX.1 d NX.2 e NX.3 f LengthX.0 g LengthX.1	176	X	X	
	b Pcfg 00 C2 c Pcfg 01 d Pcfg 02 e Pcfg 03	b Pcfg 04 C2 c Pcfg 05 d Pcfg 06 e Pcfg 07	F16	F16	b Pcfg 08 C2 c Pcfg 09 d Pcfg 10 e Pcfg 11	F16	b Pcfg 12 C2 c Pcfg 13 d Pcfg 14 e Pcfg 15	F16	b IfuBmux 12 c IfuBmux 13 d IfuBmux 14 e IfuBmux 15 f	197	X	X	
09		b ALU 00 c ALU 01 d ALU 02 e ALU 03	181	181	b ALU 04 c ALU 05 d ALU 06 e ALU 07				b ALU 08 c ALU 09 d ALU 10 e ALU 11	181	b ALU 12 c ALU 13 d ALU 14 e ALU 15	181	181
11	b Pcj 00 C0 c Pcj 01 d Pcj 02 e Pcj 03	b Pcj 04 C0 c Pcj 05 d Pcj 06 e Pcj 07	F16	F16	b Pcj 08 C0 c Pcj 09 d Pcj 10 e Pcj 11	F16	b Pcj 12 C0 c Pcj 13 d Pcj 14 e Pcj 15	F16	b dalu 08 c dalu 09 d dalu 10 e dalu 11	158	158	158	
	a PcjCarry b PcjCarry	a PcfGCarry b PcfGCarry	1660	1660			a dlnPcfG b PcfGCarry c PcjCarry d PcjLd	1664	a FH b SH	a preClk1 b preClk1	210	210	

A

B

C

D

E

F

	102	84	68	52	36	20				
01	b RcvdBmux 05 c RcvdBmux 13 d RcvdBmux 06 e RcvdBmux 14 f RcvdBmux 07 h RcvdBmux 15	195	A GenOut.11 b GenOut.10 c GenOut.09 d GenOut.08	125	A GenOut.07 b GenOut.06 c GenOut.05 d GenOut.04	125	A Genin.03 b Genin.02 c Genin.01 d Genin.00	A Genin.11 b Genin.10 c Genin.09 d Genin.08	A prepreFH'a b See Pg. 2	231
02	b dBmux 06 c dBmux 14	174	A GenOut.15 b GenOut.14 c GenOut.13 d GenOut.12	125	A GenOut.03 b GenOut.02 c GenOut.01 d GenOut.00	125	A Genin.07 b Genin.06 c Genin.05 d Genin.04	A Genin.150 b Genin.14 c Genin.13 d Genin.12	a ClkEnable b prepreDblClk	210
03	b dBmux 07 c dBmux 15	174	Spec 1 EventCntB F16	Spec 1 EventCntB F16	Spec 1 EventCntB F16	a BCntCarry b BCntCarry c BCntCarry d BCntCarry	Spec 1 EventCntA F16	Spec 1 EventCntA F16	Spec 1 EventCntA F16	Spec 1 EventCntA F16
04	CntClk BCntMuxCntrl	176	Spec 1 EventCntB F16	Spec 1 EventCntB F16	Spec 1 EventCntB F16	a ACntCarry b ACntCarry c ACntCarry d ACntCarry	a dTWReq01	212	Spec 1 EventCntA F16	Spec 1 EventCntA F16
05	CntClk ACntMuxCntrl	176	BCntMux 164	ACntMux 164		a dCntA b dCntB c dCntB d dCntB	Spec 1 EventCntA F16	DvDly MU164		
06	Temp Sensor		X	a CntClk b SpecClk1	B B 210	A IfuReset b NewGo SpecClk0	Spec 1 EventBx c EventCx d EventDx e EventEx f Miss g NotRdyImp	176	Spec 1 EventBx c EventCx d EventDx e EventEx f Miss g NotRdyImp	176
07	c0 Events	176	c0 Events 176	X	a clk0 b SpecClk0	B B 210	Misc	NK	MU164	MU164
08	a EventCntB b EventCntB c EventCntB D EventCntB	104	a BCntMuxEnb b IfuHold c ACntMuxEnb D bEmuOrFT	102	X	SpecClk0 A SyncedTTW b TWReq01	A TimeToWake b del TTW Pendulum	231	PcF	MU164
09	TwoAlphaK	415	SignK 415	NK.0 415	NK.1 415	NK.2 415	NK.3 415			
10	TypePauseK	415	Parity2 415	MEMBK.0 415	IfuAddr 3 415	MemBK.1 415	IfuAddr 0 415			
11	TypeJumpK	415	b J0a c J1a d J2a e J3a	c0 F16	b J0b c J1b d J2b e J3b	c0 F16	b J0c c J1c d J2c e J3c	c0 F16	b J0d c J1d d J2d e J3d	c0 F16 415
12	a preClk0 b preClk0	210	b J4a c J5a d J6a e J7a	c0 F16	b J4b c J5b d J6b e J7b	c0 F16	b J4c c J5c d J6c e J7c	c0 F16	b J4d c J5d d J6d e J7d	c0 F16 415

G

H

I

J

K

L

13	b H 0 c H 1 d H 2 e H 3 f H 4 g H 5 176	HC1 c d e f g 176	b H.6 c H.7 d HFault 176	HC1 c d e f g 176	b PcM 00 c PcM 01 d PcM 02 e PcM 03 f PcM 04 g PcM 05 176	MC0 b c d e f g 176	b AlphaM 0 c AlphaM 1 d AlphaM 2 e AlphaM 3 f AlphaM 4 g AlphaM 5 176	MC0 b c d e f g 176	b AlphaM 6 c AlphaM 7 d PcM 12 e PcM 13 f PcM 14 g PcM 15 176	MC0 a b c d e f g 176	a preFH b TurnOffAlu 212
14	b EnableH 0 c EnableH 1 d EnableH 2 e EnableH 3 f EnableH 4 h EnableH 5 197	a EnableH 6 b EnableH 7 c d dSignX D dTwoAlphaX 104	b PcM 06 c PcM 07 d PcM 08 e PcM 09 f PcM 10 g PcM 11 176	MC0 b c d e f g 176	b LengthM.0 c LengthM.1 d SpareM.0 e SpareM.1 f dNM = 17a g dNM = 17b 176	MC0 b c d e f g 176	b LengthM.0 c LengthM.1 d SpareM.0 e SpareM.1 f dNM = 17a g dNM = 17b 176	FGParityErr 170	b InstrSet 0a c InstrSet 0b d InstrSet 1a e InstrSet 1b FFc1 F16	170	F16
15	b Brkins 0 c2 c Brkins 1 d Brkins 2 e Brkins 3 F16	b Brkins 4 c2 c Brkins 5 d Brkins 6 e Brkins 7 F16	b SignM c TwoAlphaM d NM 0 e NM 1 f NM 2 g NM 3 176	MC0 b c d e f g 176	a NM = 17 b NK2&NK3 c NK0&NK1 d IfuMemAck 104	MC0 b c d e f g 176	a NM = 17 b NK2&NK3 c NK0&NK1 d IfuMemAck 104	a dHJ4 b dHJ5 c dHJ6 d dHJ7 1664	a InstrSetLd b CntLd C d TestOrReset 103	1664	103
16	b TestReg 0 Test1 c TestReg 1 d TestReg 2 e TestReg 3 f TestReg 4 g TestReg 5 176	b TestReg 6 Test1 c TestReg 7 d e TestFH f TestSH g Testing 176	b MemBM 0 c MemBM 1 d LengthM = 3 e MDv f TypeJumpM g LengthM = 3 176	MC0 A BrkPending b c2	a dHJ0 b dHJ1 c dHJ2 d dHJ3 231	MC0 A b c2	a dHJ0 b dHJ1 c dHJ2 d dHJ3 1664	1664	IncPcFG	119	
17	b TestIfuAck Test1 c TestMemAck d TestMakeF+D e TestFault f g 176	PipeClkEn 121	A SawFGPe c2 b (delayed clock) 231	b AlphaXLd c XShift 117	A Pause c0 b IncPcF 231	A b c0	a dPause b PcfGld c blfuHold d dAckJunkTW 1664	1664		1664	
18	b NewPc1 c AckJunkTW d DecLo+ e DecHi+ f g Brkins+ FF1 176	b GenOut+ c InstrSetOrJunk+ d IfuReset1 f g 176	a HClk1' C b TestClk1' C 210	a MClik0' C b FFClk1' C 210	a XLd b KReady 1660	a b c d 1660	InstrAddrLd 121	121			
19	a BMuxEnable B NextBeta 109	a dNewGo B EnBmuuxOut c TestLd 105	a dblclk' C b SpecClk1' C 210	a FFClik0' C b Clk0' C 210	a PcfG15 b KReady c Kready d dBrkLd 1662	a b c d 1662		212			
20	b SignX AXCO c TwoAlphaX d BetainM F16	b blfuFault c0 c NewF d NewF' e MLdDly f DoJump g DoJump' 176	b Test+ Spec1 c dTickPeriod d RamErrDly e FGErrDly f WantIfuHoldDly g 176	b ExtendH c slncPcF 117	a HDv c2 b FDv 105	a b c d 105		135			
21	A TickPeriod b ShutUp (junk) Spec1 231	b c WantIfuHold 117	b InstrSetOrJunk+ c ReschedPending d SayRamParityErr e DecLo+ f DecHi+ h TestMemAck' 195	b dJdv c ZapJ 117	b BrkLd c SayNotReady 117	a NewJ b RefOutstanding c0 135					
22	A FF130 b FF131 c FF132 d FF133 100	a dReschedPending b dReschedPending 1660	b ReschedPending c NewPc+ f/0 d WantResched e KReadyDly f GdVdly g IncPcFGDly 176	a SayResched b SayFGParityErr C BetainM' d IfuNextData 103	a BetainH B JFDv c NewGoOrNoM 105	a dSayNotReady b K NewJ c dGdv d K FDv 1664					
23	A FF134 b FF135 c FF136 d FF137 100	A FF100 b FF101 c FF102 d dReschedPending 100	FC	b GenOut+ c DMuxEnable d AckJnkTW' inv e DMuxEnable f ReschedPending' h SayNotReady 195	a ZapFGH B JHDv c SeeJump 105	a EnableFG' b DMuxEnable C dMiss d 1ByteJumpInJ 1660					
24	FB	a FF5 b FF6 c FF7 d EmuOrFT' 161	a FA = 1 b SayStuff 1664	a J↔OddF b SayNotReady1 210	a EnableFG' b DMuxEnable C dMiss d 1ByteJumpInJ 1660	a b c d e specialPcFG15 103					
	A 10	B 26	C 42	D 58	E 74	F 92					

MemB
x EmuOrFT'
x NextData
x WantIfuHold
xASEL0

XEROX PARC	Project Dorado	reference Lower Left Quadrant	File ifu21.sil	Designer S. Ornstein	Rev Cg	Date 12/21/79	Page 21
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13	a preDbIClk b PipeClkEn <i>210</i> <i>21-1</i>	A SawRamParityErr b	RamParityErr 2	RamParityErr 0	RamParityErr 1	Parity1
	<i>c0</i>	231	170	170	170	415
14	RBaseSel 415	MemB 34 415	IfuAddr 2 415	IfuAddr 4 415	IfuAddr 6 415	IfuAddr 8 415
15	LengthK.0' 415	a HDv b HDv c KReady d dGld	LengthK.1' 1662	IfuAddr 5 415	IfuAddr 7 415	IfuAddr 9 415
16	a MightBeJump B WantIfuRef c IfuMakeF->D 105	a dHDv b ZapOrJEmpty c dJdV D dSawFGPE 102	A ExceptionDispatch b	J	PcJ MU164	Top MU164
17	a dPause b c RealJFault D dWantResched 102	b JDV' c JDV d JFault e JFault' <i>c0</i> F16	Loads MU164	H MU164	b HDvDly c FDvDly d GLdDly' e GFaultDly' f ExceptionDly' <i>c0</i> 176	Bottom MU164
18	a LengthK.0 b LengthK.1 1660	FF's MU164	Dv's MU164	K MU164	Jumps MU164	Bottom MU164
19	b GDv'a c GDv' d GFault e GDv F16	c2 OtherHole 121	a clk0' D b clk0' D 210	a dblclk' D b clk1' D 210	Exception MU164	DMadr1-5 176
20	dGDv 121	WantIfuRef2 121	A 1ByteJumplnJ b 1ByteJumplnJd <i>c0</i> 135	A Mar+PcF b FFault c1 231	a WantIfuRef1 b WantIfuRef1 c WantIfuRef1 D 102	a K KillResponse b IfuAddr 6 C K RefOutstanding d IfuAddr 7 103
21	a WantIfuRef1 b WantIfuRef2 c WantIfuRef3 d WantIfuRef' 1662	dGDv 119	b FGFault c FGFault 117	a K HDv b K HDv c K HDv D Exception 102	A IfuAddr 4 b IfuAddr 9 c IfuAddr 53 d IfuAddr 12 101	A KillResponse c2 135
22	GLd 119	A dGld1 b dGld2 c Exception 106	a RealHFault b Exception' c IfuAddr 8 d IfuAddr 9 1662	a ValidRam b Exception 1660	A IfuAddr 4 b IfuAddr 9 <i>c0</i> <i>c0</i> 231	DMadr6-11 176
23	JLdb 121	a bMLd b dMiss c dAckJunkTW d 1662	b SayNotReady c dMiss 118	A IfuAddr 5 b IfuAddr 8 c IfuAddr 10 d IfuAddr 11 101	A IfuAddr 3 b IfuAddr 8 <i>c0</i> <i>c0</i> 231	A MidasGroup b DMuxClk c d IfuTrueb 101
24	MLd 121	JLda 121	A IfuAddr 1 b IfuAddr 6 <i>c0</i> 231	A IfuAddr 2 b IfuAddr 7 <i>c0</i> 231	A IfuAddr 0 b IfuAddr 5 <i>c0</i> 231	DMuxData MU164

92 **G** 110 **H** 126 **I** 142 **J** 158 **K** 174 **L**
FG0-6 IfuAddr0-9 x IfuNextMacro x WantIfuRef
MakeF->D
IfuAck
DMuxData
DMuxClock

IF Data Selector PROM SG 139 (see Dwg. 02)

N	Two Alpha	JMP	Length	Address	Contents	Numeric Sequence	Effective Sequence
N			0	00	11111111	3, 3, 3, 3, 3	IL, IL, IL, IL, IL.....
			1	01	11111111		
			2	02	11111111		
			3	03	11111111		
			0	04	11111111	2, 3, 3, 3, 3	N, IL, IL, IL, IL.....
			1	05	11110111		
			2	06	10110011		
			3	07	10010001		
			0	10	11111111	3, 3, 3, 3, 3	IL, IL, IL, IL, IL.....
			1	11	11111111		
			2	12	11111111		
			3	13	11111111		
			0	14	11111111	2, 1, 0, 3, 3	N, Alpha[0:3], Alpha[4:7], IL, IL.....
			1	15	11111111		
			2	16	10010101		
			3	17	10000100		
no N			0	20	11111111	3, 3, 3, 3, 3	IL, IL, IL, IL, IL.....
			1	21	11111111		
			2	22	11111111		
			3	23	11111111		
			0	24	11111111	0, 3, 3, 3, 3	Alpha, IL, IL, IL, IL.....
			1	25	11111111		
			2	26	01110111		
			3	27	00110011		
			0	30	11111111	0, 0, 3, 3, 3	Alpha, Beta, IL, IL, IL.....
			1	31	11111111		
			2	32	11111111		
			3	33	11111111		
			0	34	11111111	3, 3, 3, 3, 3	IL, IL, IL, IL, IL.....
			1	35	11111111		
			2	36	00111011		
			3	37	00011001		



No zero length instructions

No 3 - Byte Jumps

Jumps never export anything other than the length (no "N" on 2 - byte Jumps).

A one - byte instruction specifying Two Alpha is meaningless

Page Numbers: Yes First Page: 1
 Columns: 2 Edge Margin: .8" Between Columns: .0"
 Heading:
 IFU-mwRev-Cg.ps
 COMPONENTS:

F16:	1	2	3	4	5	6
	8	9	10	11	13	14
F415A:	6	12				
MC100:	4					
MC101:	7	8	9	11	16	
MC102:	1	2	3	4	7	13
	14					
MC103:	1	2	3	4	7	14
	16					
MC104:	1	5	6	14		
MC105:	1	2	3	4	8	11
MC106:	2	3	4	7		
MC109:	3	4				
MC117:	1	2	3	5		
MC118:	7	14				
MC119:	1	3				
MC121:	1	3	18			
MC124:	13					
MC125:	14					
MC135:	1	2	3			
MC141:	2					
MC158:	5	9	11			
MC161:	4					
MC164:	13	14				
MC1660:	1	2	3	4	6	7
	10					
MC1662:	1	2	3	4	7	9
	13	14				
MC1664:	1	2	3	4	5	10
	13	14				
MC1672:	2	9				
MC170:	5	6				
MC173:	8	9	11			
MC174:	5	8	9	11		
MC176:	1	2	3	4	5	6
	8	9	11	13	14	16
MC181:	8	9	10			
MC195:	1	2	4	7	8	9
	10	11	16			
MC197:	5	8	9	11		
MC210:	4	7				
MC212:	1	3	15			
MC231:	1	2	4	7	15	18
MU164:	16	17				
SE210:	18					
SE212:	10	18				
SG139:	2					
SIP:	13					
SPARE:	15					
TEMP:	15					

SIGNAL NAMES:

+:	1(1)	2(1)	3(1)	4(1)	5(1)	6(1)
	7(1)	8(1)	9(1)	10(1)	11(1)	12(1)
	13(1)	14(1)	15(1)	16(1)	17(1)	18(1)
AckJunkTW:	4(1)	15(1)				
AckJunkTW':	4(1)	15(1)				
AlphaX.0:	2(1)	5(2)				
AlphaX.1:	5(2)					
AlphaX.2:	5(2)					
AlphaX.3:	5(2)					
AlphaXLd:	3(1)	17(1)				
AlphaXLd':	3(1)	11(3)				
ASEL.0':	1(1)	14(1)				
bEmuOrFT:	13(1)	14(1)				
BetaInH:	2(2)	3(2)				
BetaInH':	1(1)	2(1)	3(3)			
BetaInM:	2(1)	17(1)				

BetaInM':	2(1)	3(1)		
bIfuHold:	3(4)	14(1)		
bLengthK.0':	6(1)	7(2)		
bLengthK.1':	3(1)	6(1)	7(1)	
bMLd':	2(1)	3(1)		
bMLd'%:	3(1)			
BMux.00:	8(1)			
BMux.00!:	8(1)			
BMux.01:	8(1)			
BMux.01!:	8(1)			
BMux.02:	8(1)			
BMux.02!:	8(1)			
BMux.03:	8(1)			
BMux.03!:	8(1)			
BMux.04:	8(1)			
BMux.04!:	8(1)			
BMux.05:	8(1)			
BMux.05!:	8(1)			
BMux.06:	8(1)			
BMux.06!:	8(1)			
BMux.07:	8(1)			
BMux.07!:	8(1)			
BMux.08:	9(1)			
BMux.08!:	9(1)			
BMux.09:	9(1)			
BMux.09!:	9(1)			
BMux.10:	9(1)			
BMux.10!:	9(1)			
BMux.11:	9(1)			
BMux.11!:	9(1)			
BMux.12:	9(1)			
BMux.12!:	9(1)			
BMux.13:	9(1)			
BMux.13!:	9(1)			
BMux.14:	9(1)			
BMux.14!:	9(1)			
BMux.15:	9(1)			
BMux.15!:	9(1)			
BMuxEnable:	4(1)	10(1)	11(3)	17(1)
bPipeClkEn'a:	18(3)			
bPipeClkEn'a%:	18(1)			
bPipeClkEn'b:	18(1)			
bPipeClkEn'b%:	18(1)			
bPipeClkEn'd:	18(4)			
bPipeClkEn'd%:	18(1)			
Brkins<:	3(1)	4(3)	17(1)	
BrkLd:	3(1)	17(1)		
BrkLd':	3(1)	4(1)	11(2)	
BrkPending:	1(1)	2(1)	4(1)	10(1)
BrkPending':	3(1)	4(1)		17(1)
ci1%:	10(1)			
ci2%:	10(1)			
ci3%:	10(1)			
ci4%:	10(1)			
ci5%:	10(1)			
ci6%:	10(1)			
CLK.ifu':	18(1)			
CLK.ifu'%:	18(1)			
clk0'Aa:	2(3)			
clk0'Aa%:	18(1)			
clk0'Ab:	10(3)			
clk0'Ab%:	18(1)			
clk0'Ac:	10(1)	11(2)		
clk0'Ac%:	18(1)			
clk0'Ba:	11(2)	14(1)		
clk0'Ba%:	18(1)			
clk0'Bb:	11(3)			
clk0'Bb%:	18(1)			
clk0'Bc:	11(3)			
clk0'Bc%:	18(1)			
clk0'Ca:	1(1)			
clk0'Ca%:	18(1)			
clk0'Cb:	2(1)			
clk0'Cb%:	18(1)			
clk0'Cc:	11(2)			
clk0'Cc%:	18(1)			

clk0'Da:	2(1)	7(1)	11(1)
clk0'Da%:	18(1)		
clk0'Db:	2(1)	7(2)	
clk0'Db%:	18(1)		
clk0'Dc:	7(2)		
clk0'Dc%:	18(1)		
clk0'Dd:	7(2)		
clk0'Dd%:	18(1)		
clk0'De:	7(2)		
clk0'De%:	18(1)		
clk0'Df:	7(2)	11(1)	
clk0'Df%:	18(1)		
clk1'Aa:	10(1)		
clk1'Aa%:	18(1)		
clk1'Ab:	10(2)		
clk1'Ab%:	18(1)		
clk1'Ac:	10(1)		
clk1'Ac%:	18(1)		
clk1'Da:	1(1)		
clk1'Da%:	18(1)		
CLKEnable'a!%:	18(1)		
CntClk'Ba:	13(1)		
CntClk'Ba%:	18(1)		
CntClk'Bb:	14(1)		
CntClk'Bb%:	18(1)		
CntLd':	4(1)	18(1)	
CountMiss:	14(1)		
CrryEvCntA:	13(1)		
db1Clk'Aa:	10(1)		
db1Clk'Aa%:	18(1)		
db1Clk'Ab:	10(1)		
db1Clk'Ab%:	18(1)		
db1Clk'Ac:	10(2)		
db1Clk'Ac%:	18(1)		
db1Clk'Ca!0:	10(1)		
db1Clk'Ca!1%:	18(1)		
db1Clk'Ca!2:	2(1)		
db1Clk'Ca!3:	2(1)		
db1Clk'Cb:	3(1)	4(1)	
db1Clk'Cb%:	18(1)		
db1Clk'Cc:	11(2)		
db1Clk'Cc%:	18(1)		
db1Clk'Da:	1(1)		
db1Clk'Da%:	18(1)		
db1Clk'Dc:	11(1)		
db1Clk'Dc%:	18(1)		
DecHi<':	4(1)	12(3)	
DecLo<':	4(1)	12(4)	
dGoodIfuJump:	14(2)		
dHJ.0!0%:	5(1)		
dHJ.0!1:	5(1)		
dHJ.1!0%:	5(1)		
dHJ.1!1:	5(1)		
dHJ.2!0%:	5(1)		
dHJ.2!1:	5(1)		
dHJ.3!0%:	5(1)		
dHJ.3!1:	5(1)		
dHJ.4!0%:	5(1)		
dHJ.4!1:	5(1)		
dHJ.5!0%:	5(1)		
dHJ.5!1:	5(1)		
dHJ.6!0%:	5(1)		
dHJ.6!1:	5(1)		
dHJ.7!0%:	5(1)		
dHJ.7!1:	5(1)		
dIA.04%:	7(1)		
dIA.05%:	7(1)		
dIA.06%:	7(1)		
dIA.07%:	7(1)		
dIA.08%:	7(1)		
dIA.09%:	7(1)		
DMadr.01:	16(2)		
DMadr.02:	16(3)		
DMadr.03:	16(3)		
DMadr.04:	16(3)		
DMadr.05:	16(3)		

DMadr.06:	16(3)		
DMadr.07:	16(3)		
DMadr.08:	16(3)		
DMadr.09:	16(2)	17(4)	
DMadr.10:	16(2)	17(4)	
DMadr.11:	16(2)	17(4)	
DMuxClk!:	16(1)		
DMuxData:	16(1)		
DMuxData!:	16(1)		
DoJump:	2(2)	3(2)	17(1)
DoJump':	1(1)	2(3)	3(1)
DSel0:	2(2)	3(1)	11(2)
DSel1:	2(2)	3(1)	11(2)
DSel1:	2(2)	3(1)	17(1)
EmuOnlyB':	14(2)		
EmuOrFT'!:	14(1)		
EnableFG':	5(1)	17(1)	
EnableFG'%:	1(1)		
EnBMuxOut':	4(1)	11(8)	
EnEventCntB:	4(1)	11(4)	
EventA!:	14(1)		
EventAx:	13(1)	14(1)	
EventB!:	14(1)		
EventBx:	14(2)		
EventC!:	14(1)		
EventCntA.00:	8(1)	13(1)	
EventCntA.01:	8(1)	13(1)	
EventCntA.02:	8(1)	13(1)	
EventCntA.03:	8(1)	13(1)	
EventCntA.04:	8(1)	13(1)	
EventCntA.05:	8(1)	13(1)	
EventCntA.06:	8(1)	13(1)	
EventCntA.07:	8(1)	13(1)	
EventCntA.08:	9(1)	13(1)	
EventCntA.09:	9(1)	13(1)	
EventCntA.10:	9(1)	13(1)	
EventCntA.11:	9(1)	13(1)	
EventCntA.12:	9(1)	13(1)	
EventCntA.13:	9(1)	13(1)	
EventCntA.14:	9(1)	13(1)	
EventCntA.15:	9(1)	13(1)	
EventCntB.00:	8(1)	14(1)	
EventCntB.01:	8(1)	14(1)	
EventCntB.02:	8(1)	14(1)	
EventCntB.03:	8(1)	14(1)	
EventCntB.04:	8(1)	14(1)	
EventCntB.05:	8(1)	14(1)	
EventCntB.06:	8(1)	14(1)	
EventCntB.07:	8(1)	14(1)	
EventCntB.08:	9(1)	14(1)	
EventCntB.09:	9(1)	14(1)	
EventCntB.10:	9(1)	14(1)	
EventCntB.11:	9(1)	14(1)	
EventCntB.12:	9(1)	14(1)	
EventCntB.13:	9(1)	14(1)	
EventCntB.14:	9(1)	14(1)	
EventCntB.15:	9(1)	14(1)	
EventCx:	13(1)	14(2)	
EventD!:	14(1)		
EventDx:	14(2)		
EventE!:	14(1)		
EventEx:	13(1)	14(1)	
Exception!1%:	7(1)		
Exception!2:	7(4)		
Exception!3:	16(1)	17(1)	
Exception':	7(2)		
Exception'%:	7(2)		
ExceptionDispatch:	4(1)	7(1)	
ExceptionDispatch':	7(1)	14(1)	
ExceptionDly:	16(1)	17(1)	
ExtendH:	2(1)	8(8)	
FA=1' :	4(1)		
FA=1'a:	4(5)		
FA=1'b:	4(5)		
FA=1'c:	1(2)	4(5)	
FB=0' :	4(6)		
FB=2' :	1(1)	4(1)	

FB=3':	4(3)	
FB=6':	1(1)	4(1)
FB=7':	4(3)	
FC=0':	4(3)	
FC=1':	4(3)	
FC=2':	4(3)	
FC=3':	4(3)	
FC=4':	4(4)	
FC=5':	4(2)	
FC=6':	4(2)	
FC=7':	4(2)	
FDv!0:	2(1)	3(2)
FDv!1:	1(3)	3(1)
FDv!2:	16(1)	17(1)
FDv':	1(1)	3(1)
FDvDly:	16(1)	17(1)
FF.2!:	4(1)	
FF.3!:	4(1)	
FF.4!:	4(1)	
FF.5!:	4(1)	
FF.6!:	4(1)	
FF.7!:	4(1)	
FFault':	1(2)	5(1)
FFC1k0'Cb:	11(1)	
FFC1k0'Cb%:	18(1)	
FFC1k1'Ca:	4(1)	
FFC1k1'Ca%:	18(1)	
FFC1k1'Cb:	11(1)	
FFC1k1'Cb%:	18(1)	
FFEnable':	18(8)	
FFEnable'%:	18(1)	
FG.0:	5(1)	
FG.0%:	5(1)	
FG.1:	5(1)	
FG.1%:	5(1)	
FG.2:	5(1)	
FG.2%:	5(1)	
FG.3:	5(1)	
FG.3%:	5(1)	
FG.4:	5(1)	
FG.4%:	5(1)	
FG.5:	5(1)	
FG.5%:	5(1)	
FG.6:	5(1)	
FG.6%:	5(1)	
FG.7:	5(1)	
FG.7%:	5(1)	
FG.8%:	5(1)	
FGDv:	3(2)	
FGDv':	2(1)	3(3)
FGErrDly:	2(2)	17(1)
FGFault:	5(1)	17(1)
FGFault':	5(2)	7(1)
FGParityErr'!0:	2(1)	
FGParityErr'!1:	2(1)	
FGParityErr'!2%:		5(1)
FH:	3(1)	
FH%:	18(1)	
FH'!0:	3(4)	18(1)
FH'!1%:	18(1)	
FH'!2:	1(2)	2(1) 3(1)
foo.0%:	5(1)	
foo.1%:	5(1)	
foo.2%:	5(1)	
foo.3%:	5(1)	
foo.4%:	5(1)	
foo.5%:	5(1)	
foo.6%:	5(1)	
foo.7%:	5(1)	
FullAlpha:	2(1)	11(1)
FullAlpha':	2(2)	
GDv!0:		17(1)
GDv!1:	1(2)	3(1) 5(1)
GDv!2:	3(1)	
GDv!3:	2(1)	3(2)
GDv!4:	16(1)	

GDv':	1(1)					
GDv'%:	3(1)					
GDv'a:	3(2)	5(1)				
GDvDly:	16(1)	17(1)				
GenIn.00:	13(1)					
GenIn.01:	13(1)					
GenIn.02:	13(1)					
GenIn.03:	13(1)					
GenIn.04:	13(1)					
GenIn.05:	13(1)					
GenIn.06:	13(1)					
GenIn.07:	13(1)					
GenIn.08:	13(1)					
GenIn.09:	13(1)					
GenIn.10:	13(1)					
GenIn.11:	13(1)					
GenIn.12:	13(1)					
GenIn.13:	13(1)					
GenIn.14:	13(1)					
GenIn.15:	13(1)					
GenOut.00:	14(1)					
GenOut.01:	14(1)					
GenOut.02:	14(1)					
GenOut.03:	14(1)					
GenOut.04:	14(1)					
GenOut.05:	14(1)					
GenOut.06:	14(1)					
GenOut.07:	14(1)					
GenOut.08:	14(1)					
GenOut.09:	14(1)					
GenOut.10:	14(1)					
GenOut.11:	14(1)					
GenOut.12:	14(1)					
GenOut.13:	14(1)					
GenOut.14:	14(1)					
GenOut.15:	14(1)					
GenOut<':	4(1)	14(1)	17(1)			
GFault':	1(1)	5(1)	16(1)			
GFaultDly':	16(1)	17(1)				
GLd':	3(1)	11(1)	16(1)	17(1)		
GLd'%:	3(1)					
GLdDly':	16(1)	17(1)				
Gnd:	1(1)	2(1)	3(1)	4(1)	5(1)	6(1)
	7(1)	8(1)	9(1)	10(1)	11(1)	12(1)
	13(1)	14(1)	15(1)	16(1)	17(1)	18(1)
GND:	15(1)					
GoodIfuJump:	13(1)	14(1)				
H.0:	2(1)	5(2)	9(1)	17(1)		
H.1:	5(2)	9(1)	17(1)			
H.2:	5(2)	9(1)	17(1)			
H.3:	5(2)	9(1)	17(1)			
H.4:	5(2)	9(1)	17(1)			
H.5:	5(2)	9(1)	17(1)			
H.6:	5(2)	9(1)	17(1)			
H.7:	5(2)	9(1)	17(1)			
HC1k1'Ca:	11(1)					
HC1k1'Ca%:	18(1)					
HC1k1'Cb:	11(1)					
HC1k1'Cb%:	18(1)					
HDv:	1(1)	2(1)	3(3)	16(1)	17(1)	18(1)
HDv':	1(3)	2(1)				
HDv'%:	3(1)					
HDvDly:	16(1)	17(1)				
HFault':	5(2)	7(1)	17(1)			
Hold:	13(1)	14(2)				
IfuAck:	1(1)					
IfuAddr.04'!!:	7(1)					
IfuAddr.05'!!:	7(1)					
IfuAddr.06'!!:	7(1)					
IfuAddr.07'!!:	7(1)					
IfuAddr.08'!!:	7(1)					
IfuAddr.09'!!:	7(1)					
IfuAddr.10'!!:	7(1)					
IfuAddr.11'!!:	7(1)					
IfuAddr.12'!!:	7(1)					
IfuAddr.13'!!:	7(1)					

IfuAWantsDifHit'!:	14(1)					
IfuBMux.00:	5(2)	8(1)				
IfuBMux.01:	5(2)	8(1)				
IfuBMux.02:	5(2)	8(1)				
IfuBMux.03:	5(2)	8(1)				
IfuBMux.04:	5(2)	8(1)				
IfuBMux.05:	5(2)	8(1)				
IfuBMux.06:	5(2)	8(1)				
IfuBMux.07:	5(2)	8(1)				
IfuBMux.08:	9(1)					
IfuBMux.09:	1(1)	9(1)				
IfuBMux.10:	1(1)	9(1)				
IfuBMux.11:	4(1)	9(1)				
IfuBMux.12:	4(1)	9(1)				
IfuBMux.13:	4(1)	9(1)				
IfuBMux.14:	4(1)	9(1)				
IfuBMux.15:	9(1)					
IfuData.0!:	5(1)					
IfuData.1!:	5(1)					
IfuData.2!:	5(1)					
IfuData.3!:	5(1)					
IfuData.4!:	5(1)					
IfuData.5!:	5(1)					
IfuData.6!:	5(1)					
IfuData.7!:	5(1)					
IfuFaultInEc2:	1(1)					
IfuFF.5:	4(3)					
IfuFF.6:	4(2)	11(8)				
IfuFF.7:	4(2)	11(8)				
IfuHold!1:	3(1)					
IfuHold!2:	3(1)					
IfuHold!3:	3(1)					
IfuHold!4%:	3(1)					
IfuMakeF↔D:	1(3)					
IfuMakeF↔D':	1(3)					
IfuMemAck:	1(3)					
IfuMemAck':	1(2)					
IfuMemRef:	14(2)					
IfuNextData'!:	3(3)					
IfuNextMacro'!:	3(4)					
IfuNextMacro'!%:	3(1)					
IfuRBaseSel'!:	6(1)					
IfuReset:	1(4)	3(1)	4(1)	17(1)		
IfuReset1:	3(1)	4(4)	10(1)			
IfuStartMap'!:	14(1)					
IfuTempSense:	17(1)					
IfuTempSense1:	15(1)					
IfuTrue:	1(1)	2(2)	3(3)	4(1)	10(4)	11(9)
	13(1)	14(2)	18(1)			
IfuTrueb:	11(1)					
IncPcF:	1(1)	17(1)				
IncPcF':	1(1)	10(1)				
IncPcFG'!0:	10(1)					
IncPcFG'!1:	10(2)					
IncPcFG'!1%:	10(1)					
IncPcFG'!2:	1(1)	3(1)				
IncPcFG'!3:	10(1)	16(1)	17(1)			
IncPcFGDly'!:	16(1)	17(1)				
InstrAddrK.0'!:	6(2)	7(1)	8(1)			
InstrAddrK.1'!:	6(2)	7(1)	8(1)			
InstrAddrK.2'!:	6(2)	7(1)	9(1)			
InstrAddrK.3'!:	6(2)	7(1)	9(1)			
InstrAddrK.4'!:	6(2)	7(1)	9(1)			
InstrAddrK.5'!:	6(2)	7(1)	9(1)			
InstrAddrK.6'!:	6(2)	7(1)	9(1)			
InstrAddrK.7'!:	6(2)	7(1)	9(1)			
InstrAddrK.8'!:	6(2)	7(1)	9(1)			
InstrAddrK.9'!:	6(2)	7(1)	9(1)			
InstrAddrLd:	3(1)	14(1)	17(1)			
InstrAddrLd'!:	7(6)					
InstrAddrLd'!%:	3(1)					
InstrSet.Oa:	4(1)	7(1)	12(15)			
InstrSet.Ob:	4(1)	8(1)	9(1)	12(12)	17(1)	
InstrSet.1a:	4(1)	7(1)	12(15)			
InstrSet.1b:	4(1)	8(1)	12(12)	17(1)		
InstrSetLd'!:	4(2)					

InstrSetOrJunk':	4(3)					
IOReset':	15(1)					
J.0a:	5(1)	12(7)				
J.0b:	5(1)	12(6)	17(1)			
J.0c:	5(1)	12(7)				
J.0d:	5(1)	12(7)				
J.1a:	5(1)	12(7)				
J.1b:	5(1)	12(6)	17(1)			
J.1c:	5(1)	12(7)				
J.1d:	5(1)	12(7)				
J.2a:	5(1)	12(7)				
J.2b:	5(1)	12(6)	17(1)			
J.2c:	5(1)	12(7)				
J.2d:	5(1)	12(7)				
J.3a:	5(1)	12(7)				
J.3b:	5(1)	12(6)	17(1)			
J.3c:	5(1)	12(7)				
J.3d:	5(1)	12(7)				
J.4a:	5(1)	12(7)				
J.4b:	5(1)	12(6)	17(1)			
J.4c:	5(1)	12(7)				
J.4d:	5(1)	12(7)				
J.5a:	5(1)	12(7)				
J.5b:	5(1)	12(6)	17(1)			
J.5c:	5(1)	12(7)				
J.5d:	5(1)	12(7)				
J.6a:	5(1)	12(7)				
J.6b:	5(1)	12(6)	17(1)			
J.6c:	5(1)	12(7)				
J.6d:	5(1)	12(7)				
J.7a:	5(1)	12(7)				
J.7b:	5(1)	12(6)	17(1)			
J.7c:	5(1)	12(7)				
J.7d:	5(1)	12(7)				
JDv:	3(3)	17(1)				
JDv':	1(1)	2(1)	3(3)			
JFault:	3(1)	5(1)	17(1)			
JFault':	2(1)	5(1)				
JLd'a!0:	11(4)					
JLd'a!1%:	3(1)					
JLd'a!2:	2(1)	11(4)				
JLd'b!0:	2(1)	10(2)				
JLd'b!1%:	3(1)					
JLd'b!2:	10(2)	11(1)				
JLd'b!2%:	10(1)					
JLda:	3(2)	17(1)				
JLdb:	2(1)	3(1)				
JunkTW!:	15(1)					
J+H:	1(1)	2(1)	3(2)	5(2)	10(1)	11(1)
J+H%:	1(1)					
J+H':	2(1)	5(1)				
J+H%%:	1(1)					
J+OddF:	3(1)	17(1)				
J+OddF':	3(4)					
KillResponse:	1(1)	3(1)	17(1)			
KReady:	2(2)	16(1)	17(1)			
KReady'!0:	2(1)	3(3)	7(1)			
KReady'!1:	2(1)					
KReady'!2:	1(1)	2(1)				
KReady'!3:	2(1)					
KReady'!4:	1(1)					
KReadyDly:	16(1)	17(1)				
LengthK.0:	6(1)	17(1)				
LengthK.0':	2(2)	6(2)	8(1)			
LengthK.1:	2(1)	6(1)	17(1)			
LengthK.1'!0:	8(1)					
LengthK.1'!1:	6(1)	11(2)				
LengthK.1'!2:	6(1)					
LengthK.1'!3:	1(2)	2(1)	6(1)			
LengthM.0:	2(1)	6(1)	17(1)			
LengthM.1:	2(1)	6(1)	17(1)			
LengthM=3':	2(1)	6(1)				
LengthX.0:	5(1)	6(1)	17(1)			
LengthX.1:	5(1)	6(1)	17(1)			
LengthX=3':	3(1)	6(1)				
MakeF↔D:	1(1)					

MAR.00'!:	8(1)
MAR.01'!:	8(1)
MAR.02'!:	8(1)
MAR.03'!:	8(1)
MAR.04'!:	8(1)
MAR.05'!:	8(1)
MAR.06'!:	8(1)
MAR.07'!:	8(1)
MAR.08'!:	8(1)
MAR.09'!:	9(1)
MAR.10'!:	9(1)
MAR.11'!:	9(1)
MAR.12'!:	9(1)
MAR.13'!:	9(1)
MAR.14'!:	9(1)
MAR.15'!:	9(1)
MarPcF' :	1(1) 8(4)
MC1k0'Ca:	11(3)
MC1k0'Ca%:	18(1)
MC1k0'Cb:	11(2)
MC1k0'Cb%:	18(1)
MC1k0'Cc:	11(2)
MC1k0'Cc%:	18(1)
MDv' :	1(2) 2(1) 3(2) 7(1) 17(1)
MemBK.0:	6(2) 9(1)
MemBK.1:	6(2) 9(1)
MemBK34:	6(2) 8(1)
MemBM.0!:	6(1)
MemBM.1!:	6(1)
MemBM34!:	6(1)
MemC1kEn'a:	18(1)
MemC1kEn'a!%:	18(1)
MemSH!%:	18(1)
MidasGroup0' :	16(1) 17(2)
MidasGroup1' :	16(1) 17(2)
MightBeJump:	1(1) 2(1) 3(3)
MightBeJump' :	2(2)
Miss:	13(1) 14(2)
MLd:	7(1) 17(1)
MLd%:	3(1)
MLd'!0:	3(3)
MLd'!1:	18(1)
MLd'!1%:	3(1)
MLd'!2:	1(2)
MLdDly' :	2(2) 3(1) 17(1)
MuxData0:	16(1) 17(2)
MuxData1:	16(1) 17(2)
MuxData2:	16(1) 17(2)
MuxData3:	16(1) 17(2)
MuxData4:	16(1) 17(2)
MuxData5:	16(1) 17(2)
MuxData6:	16(1) 17(2)
MuxData7:	16(1) 17(2)
NewF:	1(2) 14(1) 17(1)
NewF' :	1(5) 3(1)
NewGo:	2(3) 3(2) 4(1) 17(1)
NewGo' :	2(1) 3(1) 4(1)
NewGoOrNoM:	3(2)
NewGoOrNoM' :	3(2)
NewJ:	2(1) 17(1)
NewJ' :	2(2) 3(1)
NewPc1:	4(4)
NewPc<:	1(2) 3(1) 4(1) 17(1)
NextBeta' :	3(4)
NextData' :	3(1)
NextDataCount.0:	2(1) 8(1)
NextDataCount.1:	2(1) 8(1)
NextDataCount.2:	2(1) 8(1)
NK.0:	6(3) 9(2)
NK.0!1:	17(1)
NK.1:	6(3) 9(2)
NK.1!1:	17(1)
NK.2:	6(3) 9(2)
NK.2!1:	17(1)
NK.3:	6(3) 9(2)
NK.3!1:	17(1)

NM=17:	2(1)	6(1)	17(1)
NotReadyJump:	14(2)		
NX.0:	5(1)	6(1)	17(1)
NX.1:	5(1)	6(1)	17(1)
NX.2:	5(1)	6(1)	17(1)
NX.3:	5(1)	6(1)	17(1)
OneByteJumpInJ:	2(1)	3(2)	17(1)
OneByteJumpInJ':		2(1)	3(1)
OneByteJumpInJd:		2(1)	17(1)
OneByteJumpInJd':		2(1)	3(1)
Pause:	1(3)	17(1)	
PcF.08:	8(1)	17(1)	
PcF.09:	9(1)	17(1)	
PcF.10:	9(1)	17(1)	
PcF.11:	9(1)	17(1)	
PcF.12:	9(1)	17(1)	
PcF.13:	9(1)	17(1)	
PcF.14:	9(1)	17(1)	
PcF.15:	9(1)	17(1)	
PcFG.15%:	9(1)		
PcFG.15':	3(4)	9(1)	
PcFGCO.12':	10(3)		
PcFGCO.8':	10(2)		
PcFGLd':	3(1)	10(5)	
PcJ.08:	9(1)	17(1)	
PcJ.09:	9(1)	17(1)	
PcJ.10:	9(1)	17(1)	
PcJ.11:	9(1)	17(1)	
PcJ.12:	9(1)	17(1)	
PcJ.13:	9(1)	17(1)	
PcJ.14:	9(1)	17(1)	
PcJ.15:	9(1)	17(1)	
PcJCO.12':	10(3)		
PcJCO.8':	10(2)		
PcJLd%:	10(1)		
Pendulum!:	15(1)		
PipeC1kEn':	18(7)		
PipeC1kEn'%:	18(1)		
preC1k0'Aa:	18(1)		
preC1k0'Aa%:	18(1)		
preC1k0'Ab:	18(1)		
preC1k0'Ab%:	18(1)		
preC1k0'B:	18(2)		
preC1k0'B%:	18(1)		
preC1k0'Ca:	18(1)		
preC1k0'Ca%:	18(1)		
preC1k0'Cb:	18(2)		
preC1k0'Cb%:	18(1)		
preC1k0'D:	18(2)		
preC1k0'D%:	18(1)		
preC1k1'A:	18(1)		
preC1k1'A%:	18(1)		
preC1k1'B:	18(2)		
preC1k1'B%:	18(1)		
preC1k1'Ca:	18(2)		
preC1k1'Ca%:	18(1)		
preC1k1'Cb:	18(1)		
preC1k1'Cb%:	18(1)		
preC1k1'Cc:	18(1)		
preC1k1'Cc%:	18(1)		
preC1k1'D:	18(1)		
preC1k1'D%:	18(1)		
preDb1C1k'A:	18(1)		
preDb1C1k'A%:	18(1)		
preDb1C1k'C:	18(1)		
preDb1C1k'C%:	18(1)		
preDb1C1k'D:	18(1)		
preDb1C1k'D%:	18(1)		
PreFH:	18(3)		
PreFH%:	18(1)		
prepreDb1C1k'X%:		18(1)	
prepreDb1C1k'Y%:		18(1)	
prepreDb1C1k'Z%:		18(1)	
prepreFH%:	18(1)		
PreSH:	18(3)		
PreSH%:	18(1)		

PreSH':	18(1)
PreSH'%:	18(1)
ProcEnable':	3(6)
ProcEnable'%:	18(1)
ProcMemRef:	13(1) 14(1)
RamErrDly:	2(2) 17(1)
RamParity.0:	6(2) 8(1)
RamParity.1:	6(2) 8(1)
RamParity.2:	6(2) 8(1)
RamPe:	2(1)
RamPe%:	6(1)
RBaseSelK':	6(2) 8(1)
RcvdBMsg.00:	4(1) 6(1) 8(1) 14(1)
RcvdBMsg.00':	4(1) 8(1)
RcvdBMsg.01:	6(1) 8(1) 14(1)
RcvdBMsg.02:	6(1) 8(1) 14(1)
RcvdBMsg.03:	6(1) 8(1)
RcvdBMsg.03%:	14(1)
RcvdBMsg.04:	6(1) 8(1) 13(1) 14(1)
RcvdBMsg.05:	6(2) 8(1) 14(1)
RcvdBMsg.05%:	14(1)
RcvdBMsg.06:	4(1) 6(2) 8(1) 14(1)
RcvdBMsg.07:	4(1) 6(2) 8(1) 14(1)
RcvdBMsg.08:	6(2) 9(1) 13(1) 14(1)
RcvdBMsg.09:	6(2) 9(1) 13(1) 14(1)
RcvdBMsg.10:	6(2) 9(1) 13(1) 14(1)
RcvdBMsg.11:	6(2) 9(1) 13(1) 14(1)
RcvdBMsg.12:	6(2) 9(1) 14(2)
RcvdBMsg.13:	6(2) 9(1) 14(2)
RcvdBMsg.14:	6(2) 9(1) 14(2)
RcvdBMsg.15:	6(2) 9(1) 14(2) 15(1)
RealIJFault:	1(1) 2(2)
RealIPcFG.15:	1(1) 9(1) 17(1)
RefOutstanding:	1(3) 17(1)
RefOutstanding':	1(3)
ReschedPending:	3(1) 4(1) 7(3) 17(1)
ReschedPending':	4(2) 7(1)
SawFGParityErr:	2(1) 7(1) 17(1)
SawFGParityErr%:	7(1)
SawFGParityErr':	2(2)
SawRamParityErr:	2(1) 7(1) 17(1)
SawRamParityErr%:	7(1)
SawRamParityErr':	2(2) 7(1)
SayFGParityErrOrHigher%:	7(1)
SayNotReady:	2(1) 3(1) 7(1) 14(1) 17(1)
SayNotReadyOrHigher%:	7(1)
SayRamParityErr%:	7(1)
SayReschedOrHigher%:	7(1)
SeeJump:	2(2)
SeeJump':	2(2)
SH:	3(1)
SH%:	18(1)
SH':	1(2) 3(3) 18(1)
SH'%:	18(1)
ShutUp:	15(1)
SignIfuData:	2(1)
SignK:	2(1) 6(2) 8(1) 9(3) 17(1)
SignX':	2(1) 6(1)
SignX'!2:	17(1)
SpecClk0'Ba:	4(1) 15(1)
SpecClk0'Ba%:	18(1)
SpecClk1'Ba:	13(1)
SpecClk1'Ba%:	18(1)
SpecClk1'Bb:	14(1)
SpecClk1'Bb%:	18(1)
SpecClk1'Bc:	14(1)
SpecClk1'Bc%:	18(1)
SpecClk1'Ca:	4(1)
SpecClk1'Ca%:	18(1)
SpecClk1'Cb:	11(2)
SpecClk1'Cb%:	18(1)
SpecialSH'Aa:	11(2)
SpecialSH'Aa%:	18(1)
SpecialSH'Ab:	11(1)
SpecialSH'Ab%:	18(1)
SpecialSH'Ac:	11(1)

SpecialSH'Ac%:	18(1)			
TempRef!:	15(1)			
TestClk1'Ca:	11(1)			
TestClk1'Ca%:	18(1)			
TestClk1'Cb:	11(1)			
TestClk1'Cb%:	18(1)			
TestClk1'Cc:	11(1)			
TestClk1'Cc%:	18(1)			
TestFH':	4(1)	18(1)		
Testing:	1(3)	2(1)	4(1)	17(1)
TestLd':	4(1)	18(1)		
TestMakeF←D:	1(1)	4(1)		
TestMakeF←D!1:	17(1)			
TestSH':	4(1)	18(1)		
Test~:	4(3)	17(1)		
ThreeOutOfFive:	1(1)	17(1)		
TickPeriod':	4(1)	18(1)		
TimeToWake:	15(1)			
TTLHigh:	13(5)			
TurnOffAlu:	10(4)	17(1)		
TurnOffAlu':	10(5)			
TwoAlphaK:	6(2)	8(1)	9(1)	
TwoAlphaK!1:	17(1)			
TwoAlphaM:	2(1)	6(1)	17(1)	
TwoAlphaX:	2(1)	6(1)	17(1)	
TypeJumpK':	2(1)	3(1)	6(2)	9(1)
TypeJumpM':	2(1)	6(1)	17(1)	
TypePauseK':	1(1)	6(2)	9(1)	17(1)
ValidRam:	2(1)	3(1)	17(1)	
ValidRam':	1(2)	2(1)	6(2)	
ValidRam'%:	3(1)			
VCC:	13(1)	15(1)		
VEE:	15(1)			
WantIfuHold'!:	2(1)			
WantIfuHoldDly':		2(1)	3(1)	
WantIfuRef':	1(1)	17(1)		
WantIfuRef'%:	1(1)			
WantResched:	4(1)	17(1)		
Whatever:	15(2)			
XC1k0'Aa:	11(1)			
XC1k0'Aa%:	18(1)			
XC1k0'Ab:	11(1)			
XC1k0'Ab%:	18(1)			
XC1k0'Ac:	11(2)			
XC1k0'Ac%:	18(1)			
XLd:	2(1)	3(1)	6(2)	14(2)
XLd!2:	17(1)			
XLd'!0%:	3(1)			
XLd'!1:	4(1)			
XLd'!2:	2(3)	18(1)		
XShift':	2(3)	3(1)		
ZapFGH:	2(1)	3(3)	17(1)	
ZapFGH':	1(1)	2(1)	3(1)	10(1)
ZapJ:	2(1)	3(1)	7(1)	17(1)
ZapJ':	2(2)			
ZapOrJEmpty':	1(1)	3(3)		